EPSON

SED1565 Series

LCD driver with RAM

Technical Manual

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

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SED1500 Series
Selection Guide

■ LCD drivers with RAM for small- and medium-sized displays

Ultra-low power consumption and on-chip RAM make this series ideal for compact LCD-based equipment.

SED1500 series

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1510D0C	0.9–6.0	1.8–6.0	1/4	32	4	128	Serial	18 (internal)	Al pad chip	Small segment-type LCD display. Command and data interface
SED1510D0B									Au bump chip	
SED1510F0C									QFP12-48pin	
SED1510F0E									QFP6-60pin	
SED1511D0A									Al pad chip	Small segment-type LCD dislays. Data only interface
SED1520D0A	2.4–7.0	3.5–13	1/16,1/32	61	16	2,560	8-bit parallel	18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1520D0B									Au bump chip	
SED1520F0A									QFP5-100pin	
SED1520F0C									QFP15-100pin	
SED1520T0A									TCP	
SED1520DAA								2 (external)	Al pad chip	
SED1520DAB									Au bump chip	
SED1520FAA									QFP5-100pin	
SED1520FAC									QFP15-100pin	
SED1520TAA#									TCP	
SED1521D0A			1/8–1/32	80	–			18 (external)	Al pad chip	Extension driver for the SED1520 and SED1522
SED1521D0B									Au bump chip	
SED1521F0A									QFP5-100pin	
SED1521F0C									QFP15-100pin	
SED1521T0A#									TCP	
SED1521DAA								2 (external)	Al pad chip	
SED1521DAB									Au bump chip	
SED1521FAA									QFP5-100pin	
SED1521FAC									QFP15-100pin	
SED1521TAA#									TCP	
SED152AD0A									Al pad chip	P-substrate version of SED1521
SED1522D0A			1/8,1/16	69	8			18 (internal, external)	Al pad chip	Dot-matrix LCD displays Extension driver is the SED1521.
SED1522D0B									Au bump chip	
SED1522F0A									QFP5-100pin	
SED1522F0C									QFP15-100pin	
SED1522T0A#									TCP	
SED1522DAA								2 (external)	Al pad chip	
SED1522DAB									Au bump chip	
SED1522FAA									QFP5-100pin	
SED1522FAC									QFP15-100pin	
SED1522TAA#									TCP	
SED1540D0A		3.5–11	1/3,1/4	73	3, 4			18 (internal) 4 (external)	Al pad chip	Segment-type displays
SED1540D0B									Au bump chip	
SED1540F0A									QFP5-100pin	

: Planning TCP : Tape Carrier Package

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1560D0A	2.4–6.0	6.0–16.0	1/48, 1/49 1/64, 1/65	102	65	166×65 bits	8-bit parallel or Serial	18	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1560✻0B (1/9 bias) SED1560✻AB (1/7 bias) SED1561✻0B (1/7 bias) SED1561✻AB (1/5 bias)
SED1560DAA									Al pad chip	
SED1560D0B									Au bump chip	
SED1560DAB									Au bump chip	
SED1560T0B									TCP	
SED1560TQA									QTCP	
SED1561D0A			1/24, 1/25 1/32, 1/33	134	33				Al pad chip	
SED1561DAA									Al pad chip	
SED1561D0B									Au bump chip	
SED1561DAB									Au bump chip	
SED1561T0B									TCP	
SED1561TAB									TCP	
SED1561TQA									QTCP	
SED1562D0A			1/16, 1/17 (1/5bias)	150	17				Al pad chip	
SED1562D0B									Au bump chip	
SED1562T0B									TCP	
SED1562TQA									QTCP	
SED1565D0B	1.8–5.5	4.5–16.0	1/65 (1/7, 1/9 bias)	132	65	132×65 bits		33	Au bump chip	Built-in power circuit for LCD (DC/DC×4)
SED1565D1B*									Au bump chip	
SED1565D2B									Au bump chip	
SED1565T0A									TCP	
SED1565T0B									TCP	
SED1565T0C									TCP	
SED1566D0B			1/49 (1/6, 1/8 bias)		49				Au bump chip	
SED1566D1B*									Au bump chip	
SED1566D2B									Au bump chip	
SED1566T0A									TCP	
SED1567D0B			1/33 (1/5, 1/6 bias)		33				Au bump chip	
SED1567D1B*									Au bump chip	
SED1567D2B									Au bump chip	
SED1567T0B									TCP	
SED1567T0C									TCP	
SED1568D0B			1/55 (1/6, 1/8 bias)		55				Au bump chip	
SED1569D0B			1/53 (1/6, 1/8 bias)		53				Au bump chip	
SED1569T**									TCP	
SED1570D0A	2.7–5.5	8.0–20.0	1/64–1/200	80	–	200×80 bits	4-bit parallel	–	Al pad chip	Built-in self-refreshing function
SED1570D0B									Au bump chip	
SED1526D*A	2.4–6.0	3.5– Supply ×3 voltage	1/8, 1/9 1/16, 1/17		17	80×33 bits	8-bit parallel or Serial	20	Al pad chip	Built-in power circuit for LCD (voltage tripler) SED1526✻0✻ (VREG) SED1526✻E✻ (no VREG) SED1526✻A✻ (redistribution of COMS) SED1528✻0✻ (VREG) SED1528✻E✻ (no VREG)
SED1526D*B									Au bump chip	
SED1526F*A									QFP5-128pin	
SED1526T*A									TCP	
SED1528D*A			1/32, 1/33	64	33				Al pad chip	
SED1528D*B									Au bump chip	
SED1528F*A									QFP5-128pin	
SED1528T*A									TCP	

Part number	Supply voltage range (V)	LCD voltage range (V)	Duty	Segment	Common	Display RAM (bits)	Microprocessor interface	Frequency (KHz)	Package	Application/additional features
SED1530D0A	2.4–6.0	4.5–16.0	1/32, 1/33	100	33	132×65 bits	8-bit parallel or Serial	–	Al pad chip	Built-in power circuit for LCD (voltage quadrupler) SED153**0* (Common: Right side) SED153**A* (Common: Both side) SED153**B* (Common: Left side) SED153**F* (no VREG)
SED1530DAA									Al pad chip	
SED1530D0B									Au bump chip	
SED1530DAB									Au bump chip	
SED1530TAA									TCP	
SED1531D0A			1/64, 1/65	132	–				Al pad chip	
SED1531D0B									Au bump chip	
SED1531T0A									TCP	
SED1532D0A				100	33				Al pad chip	
SED1532DBA									Al pad chip	
SED1532D0B									Au bump chip	
SED1532DBA									Au bump chip	
SED1532T0A									TCP	
SED1532TBA									TCP	
SED1535D0B*			1/35	98	35				Au bump chip	

TCP : Tape Carrier Package

8. SED1565 Series

(Rev. 1.2)

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GENERAL DESCRIPTION

The SED1565 Series is a series of single-chip dot matrix liquid crystal display drivers that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a liquid crystal drive signal independent of the microprocessor. Because the chips in the SED1565 Series contain 65 × 132 bits of display data RAM and there is a 1-to-1 correspondence between the liquid crystal panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom.

The SED1565 Series chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65 × 132 dot display (capable of displaying 8 columns × 4 rows of a 16 × 16 dot kanji font). The SED1567 Series chips contain 33 common output circuits and 132 segment output circuits, so that a single chip can drive 33 × 132 dot display (capable of displaying 8 columns × 2 rows of 16 × 16 dot kanji fonts). Thanks to the built-in 55 common output circuits and 132 segment output circuits, the SED1568*** is capable of displaying 55 × 132 dots (11 columns × 4 lines using 11 × 12 dots Kanji font) with a single chip. The SED1569 Series chips contain 53 common output circuits and 132 segment output circuits, so that a single chip can drive 53 × 132 dot display (capable of displaying 11 columns × 4 rows of 11 × 12 dot kanji fonts). Moreover, the capacity of the display can be extended through the use of master/slave structures between chips.

The chips are able to minimize power consumption because no external operating clock is necessary for the display data RAM read/write operation. Furthermore, because each chip is equipped internally with a low-power liquid crystal driver power supply, resistors for liquid crystal driver power voltage adjustment and a display clock CR oscillator circuit, the SED1565 Series chips can be used to create the lowest power display system with the fewest components for high-performance portable devices.

FEATURES

- Direct display of RAM data through the display data RAM.
  RAM bit data: "1" Non-illuminated
  "0" Illuminated
  (during normal display)
- RAM capacity
  65 × 132 = 8580 bits
- Display driver circuits
  SED1565***: 65 common output and 132 segment outputs
  SED1566***: 49 common output and 132 segment outputs
  SED1567***: 33 common outputs and 132 segment outputs
  SED1568***: 55 common outputs and 132 segment outputs
  SED1569***: 53 common outputs and 132 segment outputs
- High-speed 8-bit MPU interface (The chip can be connected directly to the both the 80x86 series MPUs and the 68000 series MPUs)
  /Serial interfaces are supported.
- Abundant command functions
  Display data Read/Write, display ON/OFF, Normal/Reverse display mode, page address set, display start line set, column address set, status read, display all points ON/OFF, LCD bias set, electronic volume, read/modify/write, segment driver direction select, power saver, static indicator, common output status select, V5 voltage regulation internal resistor ratio set.
- Static drive circuit equipped internally for indicators. (1 system, with variable flashing speed.)
- Low-power liquid crystal display power supply circuit equipped internally.
  Booster circuit (with Boost ratios of Double/Triple/Quad, where the step-up voltage reference power supply can be input externally)
  High-accuracy voltage adjustment circuit (Thermal gradient –0.05%/°C or –0.2%/°C or external input)
  V_5 voltage regulator resistors equipped internally, V_1 to V_4 voltage divider resistors equipped internally, electronic volume function equipped internally, voltage follower.
- CR oscillator circuit equipped internally (external clock can also be input)
- Extremely low power consumption
  Operating power when the built-in power supply is used (an example)
  SED1565D0B 81 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Quad voltage, $V_5 – V_{DD}$ = –11.0 V)
  SED1566D0B 43 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1567D0B 29 μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  SED1568D0B/SED1569D0B 46μA ($V_{DD} – V_{SS} = V_{DD} – V_{SS2}$ = 3.0 V, Triple voltage, $V_5 – V_{DD}$ = –8.0 V)
  Conditions: When all displays are in white and the normal mode is selected (see page 60 *12 for details of the conditions).
- Power supply
  Operable on the low 1.8 voltage
  Logic power supply $V_{DD} – V_{SS}$ = 1.8 V to –5.5 V
  Boost reference voltage: $V_{DD} – V_{SS2}$ = 1.8 V to –6.0 V
  Liquid crystal drive power supply: $V_{DD} – V_5$ = –4.5 V to –16.0 V
- Wide range of operating temperatures: –40 to 85°C
- CMOS process
- Shipping forms include bare chip and TCP.
- These chips not designed for resistance to light or resistance to radiation.

Series Specifications

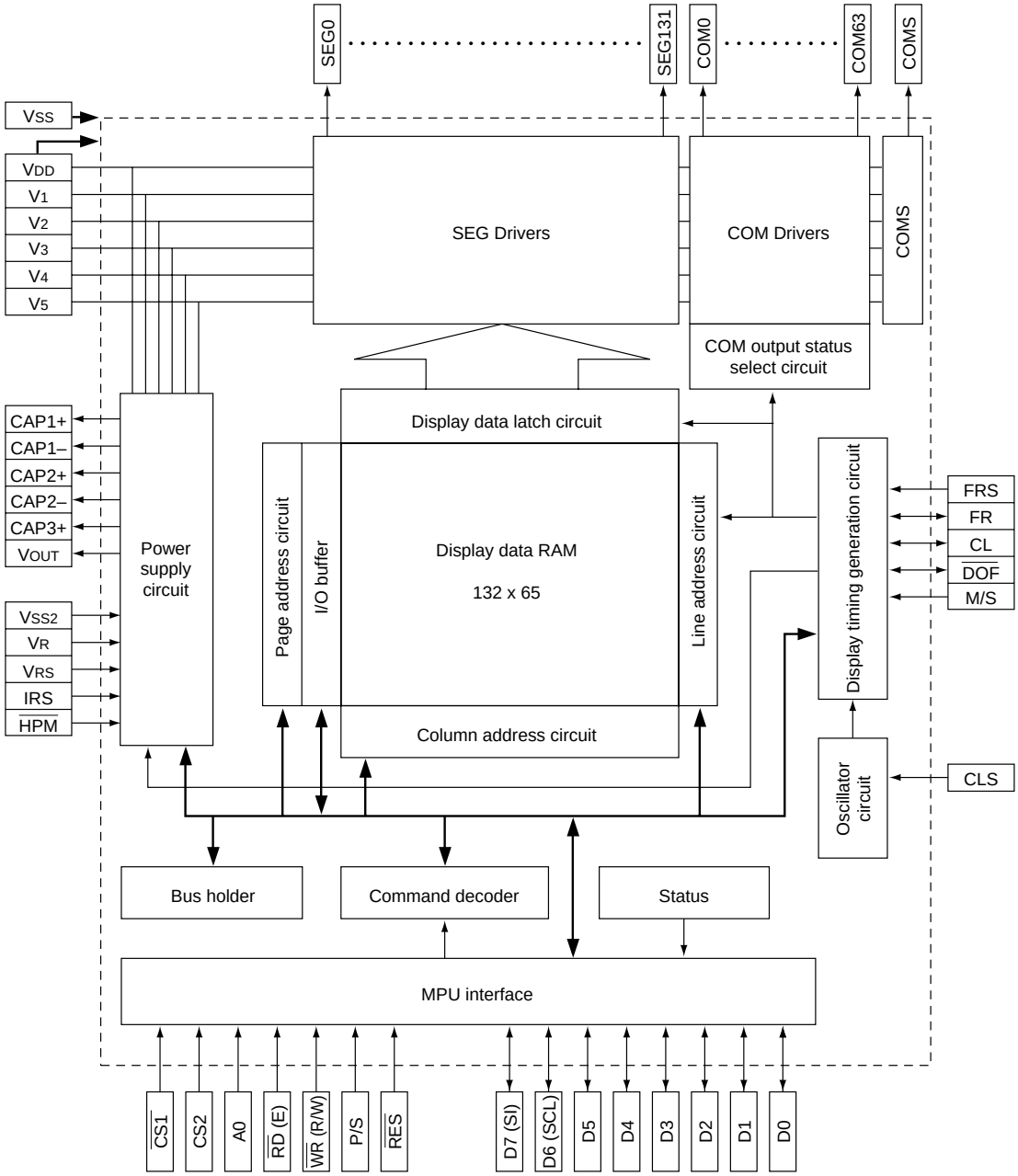
Product Name	Duty	Bias	SED Dr	COM Dr	V_{REG} Temperature Gradient	Shipping Forms
SED1565D0*	1/65	1/9, 1/7	132	65	–0.05%/°C	Bare Chip
SED1565T0*	1/65	1/9, 1/7	132	65	–0.05%/°C	TCP
* SED1565D1*	1/65	1/9, 1/7	132	65	–0.2%/°C	Bare Chip
* SED1565T1*	1/65	1/9, 1/7	132	65	–0.2%/°C	TCP
SED1565D2*	1/65	1/9, 1/7	132	65	External Input	Bare Chip
SED1565T2*	1/65	1/9, 1/7	132	65	External Input	TCP
SED1566D0*	1/49	1/8, 1/6	132	49	–0.05%/°C	Bare Chip
SED1566T0*	1/49	1/8, 1/6	132	49	–0.05%/°C	TCP
* SED1566D1*	1/49	1/8, 1/6	132	49	–0.2%/°C	Bare Chip
* SED1566T1*	1/49	1/8, 1/6	132	49	–0.2%/°C	TCP
SED1566D2*	1/49	1/8, 1/6	132	49	External Input	Bare Chip
SED1566T2*	1/49	1/8, 1/6	132	49	External Input	TCP
SED1567D0*	1/33	1/6, 1/5	132	33	–0.05%/°C	Bare Chip
SED1567T0*	1/33	1/6, 1/5	132	33	–0.05%/°C	TCP
* SED1567D1*	1/33	1/6, 1/5	132	33	–0.2%/°C	Bare Chip
* SED1567T1*	1/33	1/6, 1/5	132	33	–0.2%/°C	TCP
SED1567D2*	1/33	1/6, 1/5	132	33	External Input	Bare Chip
SED1567T2*	1/33	1/6, 1/5	132	33	External Input	TCP
SED1568D0*	1/55	1/8, 1/6	132	55	–0.05%/°C	Bare Chip
SED1569D0*	1/53	1/8, 1/6	132	53	–0.05%/°C	Bare Chip
* SED1569T0*	1/53	1/8, 1/6	132	53	–0.05%/°C	TCP

Note: The circuit for the V_{REG} temperature gradient –0.2%/°C and the external input is under preparation.

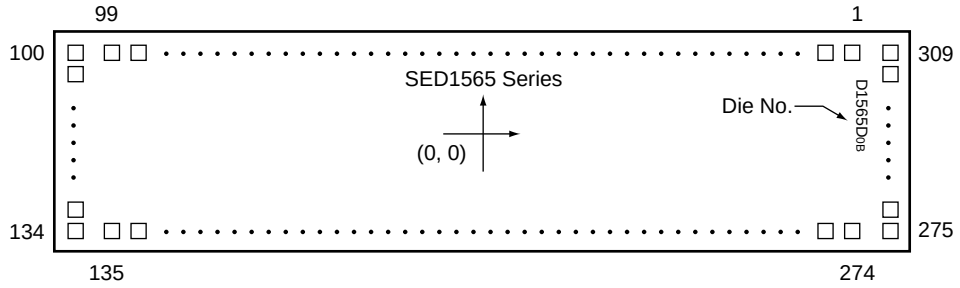
* : Under development

BLOCK DIAGRAM

Example: SED1565***



PIN DIMENSIONS



Chip Size	10.82 mm × 2.81 mm	
Bump Pitch	71 µm (Min.)	
Bump Size	PAD No. 1~24	85 µm × 85 µm
	PAD No. 25~82	64 µm × 85 µm
	PAD No. 83~99	85 µm × 85 µm
	PAD No. 100	85 µm × 73 µm
	PAD No. 101~133	85 µm × 47 µm
	PAD No. 134	85 µm × 73 µm
	PAD No. 135	73 µm × 85 µm
	PAD No. 136~273	47 µm × 85 µm
	PAD No. 274	73 µm × 85 µm
	PAD No. 275	85 µm × 73 µm
	PAD No. 276~308	85 µm × 47 µm
	PAD No. 309	85 µm × 73 µm
Bump Height	17 µm (Typ.)	
Chip Thickness	625 µm	

SED1565*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM31		1163
102	COM30		1090
103	COM29		1017
104	COM28		945
105	COM27		872
106	COM26		799
107	COM25		727
108	COM24		654
109	COM23		581
110	COM22		509
111	COM21		436
112	COM20		363
113	COM19		291
114	COM18		218
115	COM17		145
116	COM16		73
117	COM15		0
118	COM14		–73
119	COM13		–145
120	COM12		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM11	–5252	–291
122	COM10		–363
123	COM9		–436
124	COM8		–509
125	COM7		–581
126	COM6		–654
127	COM5		–727
128	COM4		–800
129	COM3		–872
130	COM2		–945
131	COM1		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM32		–1163
277	COM33		–1090
278	COM34		–1018
279	COM35		–945
280	COM36		–872

PAD No.	PIN Name	X	Y
281	COM37	5252	–800
282	COM38		–727
283	COM39		–654
284	COM40		–581
285	COM41		–509
286	COM42		–436
287	COM43		–363
288	COM44		–291
289	COM45		–218
290	COM46		–145
291	COM47		–73
292	COM48		0
293	COM49		73
294	COM50		145
295	COM51		218
296	COM52		291
297	COM53		363
298	COM54		436
299	COM55		509
300	COM56		581
301	COM57		654
302	COM58		727
303	COM59		799
304	COM60		872
305	COM61		945
306	COM62		1017
307	COM63		1090
308	COMS		1163
309	(NC)		1248

SED1566*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	HPM	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	(NC)		1090
103	COM23		1017
104	(NC)		945
105	COM22		872
106	(NC)		799
107	COM21		727
108	COM20		654
109	COM19		581
110	COM18		509
111	COM17		436
112	COM16		363
113	COM15		291
114	COM14		218
115	COM13		145
116	COM12		73
117	COM11		0
118	COM10		–73
119	COM9		–145
120	COM8		–218

Units: µm

PAD No.	PIN Name	X	Y
121	COM7	–5252	–291
122	COM6		–363
123	COM5		–436
124	COM4		–509
125	COM3		–581
126	COM2		–654
127	COM1		–727
128	(NC)		–800
129	COM0		–872
130	(NC)		–945
131	COMS		–1018
132	(NC)		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	(NC)		–1090
278	COM24		–1018
279	(NC)		–945
280	COM25		–872

PAD No.	PIN Name	X	Y
281	(NC)	5252	–800
282	COM26		–727
283	COM27		–654
284	COM28		–581
285	COM29		–509
286	COM30		–436
287	COM31		–363
288	COM32		–291
289	COM33		–218
290	COM34		–145
291	COM35		–73
292	COM36		0
293	COM37		73
294	COM38		145
295	COM39		218
296	COM40		291
297	COM41		363
298	COM42		436
299	COM43		509
300	COM44		581
301	COM45		654
302	COM46		727
303	(NC)		799
304	COM47		872
305	(NC)		945
306	COMS		1017
307	(NC)		1090
308	(NC)		1163
309	(NC)		1248

SED1567*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	COM15		1163
102	COM15		1090
103	COM14		1017
104	COM14		945
105	COM13		872
106	COM13		799
107	COM12		727
108	COM12		654
109	COM11		581
110	COM11		509
111	COM10		436
112	COM10		363
113	COM9		291
114	COM9		218
115	COM8		145
116	COM8		73
117	COM7		0
118	COM7		–73
119	COM6		–145
120	COM6		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM5	–5252	–291
122	COM5		–363
123	COM4		–436
124	COM4		–509
125	COM3		–581
126	COM3		–654
127	COM2		–727
128	COM2		–800
129	COM1		–872
130	COM1		–945
131	COM0		–1018
132	COM0		–1090
133	COMS		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	COM16		–1163
277	COM16		–1090
278	COM17		–1018
279	COM17		–945
280	COM18		–872

PAD No.	PIN Name	X	Y
281	COM18	5252	–800
282	COM19		–727
283	COM19		–654
284	COM20		–581
285	COM20		–509
286	COM21		–436
287	COM21		–363
288	COM22		–291
289	COM22		–218
290	COM23		–145
291	COM23		–73
292	COM24		0
293	COM24		73
294	COM25		145
295	COM25		218
296	COM26		291
297	COM26		363
298	COM27		436
299	COM27		509
300	COM28		581
301	COM28		654
302	COM29		727
303	COM29		799
304	COM30		872
305	COM30		945
306	COM31		1017
307	COM31		1090
308	COMS		1163
309	(NC)		1248

SED1568*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM26		1090
103	(NC)		1017
104	COM25		945
105	COM25		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: µm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM27		–1090
278	(NC)		–1018
279	COM28		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM29	5252	–800
282	COM30		–727
283	COM31		–654
284	COM32		–581
285	COM33		–509
286	COM34		–436
287	COM35		–363
288	COM36		–291
289	COM37		–218
290	COM38		–145
291	COM39		–73
292	COM40		0
293	COM41		73
294	COM42		145
295	COM43		218
296	COM44		291
297	COM45		363
298	COM46		436
299	COM47		509
300	COM48		581
301	COM48		654
302	COM50		727
303	COM51		799
304	COM52		872
305	COM53		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

SED1569*** Pad Center Coordinates

Units: μm

PAD No.	PIN Name	X	Y
1	(NC)	4973	1246
2	FRS	4853	
3	FR	4734	
4	CL	4614	
5	$\overline{DOF}$	4494	
6	TEST0	4375	
7	V_{SS}	4255	
8	$\overline{CS1}$	4136	
9	CS2	4016	
10	V_{DD}	3896	
11	$\overline{RES}$	3777	
12	A0	3657	
13	V_{SS}	3538	
14	$\overline{WR}$, R/$\overline{W}$	3418	
15	$\overline{RD}$, E	3298	
16	V_{DD}	3179	
17	D0	3059	
18	D1	2940	
19	D2	2820	
20	D3	2700	
21	D4	2581	
22	D5	2461	
23	D6, SCL	2342	
24	D7, SI	2222	
25	(NC)	2119	
26	V_{DD}	2030	
27	V_{DD}	1941	
28	V_{DD}	1852	
29	V_{DD}	1763	
30	V_{SS}	1674	
31	V_{SS}	1585	
32	V_{SS}	1496	
33	V_{SS2}	1407	
34	V_{SS2}	1318	
35	V_{SS2}	1229	
36	V_{SS2}	1140	
37	(NC)	1051	
38	V_{OUT}	962	
39	V_{OUT}	873	
40	CAP3–	784	

PAD No.	PIN Name	X	Y
41	CAP3–	695	1246
42	(NC)	605	
43	CAP1+	516	
44	CAP1+	427	
45	CAP1–	338	
46	CAP1–	249	
47	CAP2–	160	
48	CAP2–	71	
49	CAP2+	–18	
50	CAP2+	–107	
51	V_{SS}	–196	
52	V_{SS}	–285	
53	V_{RS}	–374	
54	V_{RS}	–463	
55	V_{DD}	–552	
56	V_{DD}	–641	
57	V_1	–730	
58	V_1	–819	
59	V_2	–908	
60	V_2	–997	
61	(NC)	–1086	
62	V_3	–1176	
63	V_3	–1265	
64	V_4	–1354	
65	V_4	–1443	
66	V_5	–1532	
67	V_5	–1621	
68	(NC)	–1710	
69	V_R	–1799	
70	V_R	–1888	
71	V_{DD}	–1977	
72	V_{DD}	–2066	
73	TEST1	–2155	
74	TEST1	–2244	
75	TEST2	–2333	
76	TEST2	–2422	
77	(NC)	–2511	
78	TEST3	–2600	
79	TEST3	–2689	
80	TEST4	–2778	

PAD No.	PIN Name	X	Y
81	TEST4	–2867	1246
82	(NC)	–2957	
83	V_{DD}	–3059	
84	M/S	–3179	
85	CLS	–3298	
86	V_{SS}	–3418	
87	C86	–3538	
88	P/S	–3657	
89	V_{DD}	–3777	
90	$\overline{HPM}$	–3896	
91	V_{SS}	–4016	
92	IRS	–4136	
93	V_{DD}	–4255	
94	TEST5	–4375	
95	TEST6	–4494	
96	TEST7	–4614	
97	TEST8	–4734	
98	TEST9	–4853	
99	(NC)	–4973	
100	(NC)	–5252	1248
101	(NC)		1163
102	COM25		1090
103	(NC)		1017
104	COM24		945
105	(NC)		872
106	COM23		799
107	COM22		727
108	COM21		654
109	COM20		581
110	COM19		509
111	COM18		436
112	COM17		363
113	COM16		291
114	COM15		218
115	COM14		145
116	COM13		73
117	COM12		0
118	COM11		–73
119	COM10		–145
120	COM9		–218

Units: μm

PAD No.	PIN Name	X	Y
121	COM8	–5252	–291
122	COM7		–363
123	COM6		–436
124	COM5		–509
125	COM4		–581
126	COM3		–654
127	COM2		–727
128	COM1		–800
129	(NC)		–872
130	COM0		–945
131	(NC)		–1018
132	COMS		–1090
133	(NC)		–1163
134	(NC)		–1248
135	(NC)	–5009	–1246
136	(NC)	–4924	
137	(NC)	–4853	
138	(NC)	–4781	
139	SEG0	–4709	
140	SEG1	–4637	
141	SEG2	–4565	
142	SEG3	–4493	
143	SEG4	–4421	
144	SEG5	–4349	
145	SEG6	–4277	
146	SEG7	–4206	
147	SEG8	–4134	
148	SEG9	–4062	
149	SEG10	–3990	
150	SEG11	–3918	
151	SEG12	–3846	
152	SEG13	–3774	
153	SEG14	–3702	
154	SEG15	–3630	
155	SEG16	–3559	
156	SEG17	–3487	
157	SEG18	–3415	
158	SEG19	–3343	
159	SEG20	–3271	
160	SEG21	–3199	

PAD No.	PIN Name	X	Y
161	SEG22	–3127	–1246
162	SEG23	–3055	
163	SEG24	–2983	
164	SEG25	–2912	
165	SEG26	–2840	
166	SEG27	–2768	
167	SEG28	–2696	
168	SEG29	–2624	
169	SEG30	–2552	
170	SEG31	–2480	
171	SEG32	–2408	
172	SEG33	–2336	
173	SEG34	–2265	
174	SEG35	–2193	
175	SEG36	–2121	
176	SEG37	–2049	
177	SEG38	–1977	
178	SEG39	–1905	
179	SEG40	–1833	
180	SEG41	–1761	
181	SEG42	–1689	
182	SEG43	–1618	
183	SEG44	–1546	
184	SEG45	–1474	
185	SEG46	–1402	
186	SEG47	–1330	
187	SEG48	–1258	
188	SEG49	–1186	
189	SEG50	–1114	
190	SEG51	–1042	
191	SEG52	–971	
192	SEG53	–899	
193	SEG54	–827	
194	SEG55	–755	
195	SEG56	–683	
196	SEG57	–611	
197	SEG58	–539	
198	SEG59	–467	
199	SEG60	–395	
200	SEG61	–324	

PAD No.	PIN Name	X	Y
201	SEG62	–252	–1246
202	SEG63	–180	
203	SEG64	–108	
204	SEG65	–36	
205	SEG66	36	
206	SEG67	108	
207	SEG68	180	
208	SEG69	252	
209	SEG70	324	
210	SEG71	395	
211	SEG72	467	
212	SEG73	539	
213	SEG74	611	
214	SEG75	683	
215	SEG76	755	
216	SEG77	827	
217	SEG78	899	
218	SEG79	971	
219	SEG80	1042	
220	SEG81	1114	
221	SEG82	1186	
222	SEG83	1258	
223	SEG84	1330	
224	SEG85	1402	
225	SEG86	1474	
226	SEG87	1546	
227	SEG88	1618	
228	SEG89	1689	
229	SEG90	1761	
230	SEG91	1833	
231	SEG92	1905	
232	SEG93	1977	
233	SEG94	2049	
234	SEG95	2121	
235	SEG96	2193	
236	SEG97	2265	
237	SEG98	2336	
238	SEG99	2408	
239	SEG100	2480	
240	SEG101	2552	

Units: µm

PAD No.	PIN Name	X	Y
241	SEG102	2624	–1246
242	SEG103	2696	
243	SEG104	2768	
244	SEG105	2840	
245	SEG106	2912	
246	SEG107	2983	
247	SEG108	3055	
248	SEG109	3127	
249	SEG110	3199	
250	SEG111	3271	
251	SEG112	3343	
252	SEG113	3415	
253	SEG114	3487	
254	SEG115	3558	
255	SEG116	3630	
256	SEG117	3702	
257	SEG118	3774	
258	SEG119	3846	
259	SEG120	3918	
260	SEG121	3990	
261	SEG122	4062	
262	SEG123	4134	
263	SEG124	4206	
264	SEG125	4277	
265	SEG126	4349	
266	SEG127	4421	
267	SEG128	4493	
268	SEG129	4565	
269	SEG130	4637	
270	SEG131	4709	
271	(NC)	4781	
272	(NC)	4853	
273	(NC)	4924	
274	(NC)	5009	
275	(NC)	5252	–1248
276	(NC)		–1163
277	COM26		–1090
278	(NC)		–1018
279	COM27		–945
280	(NC)		–872

PAD No.	PIN Name	X	Y
281	COM28	5252	–800
282	COM29		–727
283	COM30		–654
284	COM31		–581
285	COM32		–509
286	COM33		–436
287	COM34		–363
288	COM35		–291
289	COM36		–218
290	COM37		–145
291	COM38		–73
292	COM39		0
293	COM40		73
294	COM41		145
295	COM42		218
296	COM43		291
297	COM44		363
298	COM45		436
299	COM46		509
300	COM47		581
301	COM48		654
302	COM49		727
303	COM50		799
304	(NC)		872
305	COM51		945
306	(NC)		1017
307	COMS		1090
308	(NC)		1163
309	(NC)		1248

PIN DESCRIPTIONS

Power Supply Pins

Pin Name	I/O	Function	No. of Pins
V_{DD}	Power Supply	Shared with the MPU power supply terminal V_{CC}.	13
V_{SS}	Power Supply	This is a 0V terminal connected to the system GND.	9
V_{SS2}	Power Supply	This is the reference power supply for the step-up voltage circuit for the liquid crystal drive.	4
V_{RS}	Power Supply	This is the externally-input VREG power supply for the LCD power supply voltage regulator. These are only enabled for the models with the VREG external input option.	2
V_1, V_2, V_3, V_4, V_5	Power Supply	This is a multi-level power supply for the liquid crystal drive. The voltage applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on VDD, and must maintain the relative magnitudes shown below. $V_{DD} (= V_0) \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$ Master operation: When the power supply turns ON, the internal power supply circuits produce the V1 to V4 voltages shown below. The voltage settings are selected using the LCD bias set command.	10

	SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
V_1	1/9•V_5 1/7•V_5	1/8•V_5 1/6•V_5	1/6•V_5 1/5•V_5	1/8•V_5 1/6•V_5	1/8•V_5 1/6•V_5
V_2	2/9•V_5 2/7•V_5	2/8•V_5 2/6•V_5	2/6•V_5 2/5•V_5	2/8•V_5 2/6•V_5	2/8•V_5 2/6•V_5
V_3	7/9•V_5 5/7•V_5	6/8•V_5 4/6•V_5	4/6•V_5 3/5•V_5	6/8•V_5 4/6•V_5	6/8•V_5 4/6•V_5
V_4	8/9•V_5 6/7•V_5	7/8•V_5 5/6•V_5	5/6•V_5 4/5•V_5	7/8•V_5 5/6•V_5	7/6•V_5 5/6•V_5

LCD Power Supply Circuit Terminals

Pin Name	I/O	Function	No. of Pins
CAP1+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1- terminal.	2
CAP1–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
CAP2+	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2- terminal.	2
CAP2–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2+ terminal.	2
CAP3–	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1+ terminal.	2
V_{OUT}	O	DC/DC voltage converter. Connect a capacitor between this terminal and V_{SS}.	2
V_R	I	Output voltage regulator terminal. Provides the voltage between V_{DD} and V5 through a resistive voltage divider. These are only enabled when the V_5 voltage regulator internal resistors are not used (IRS = “L”). These cannot be used when the V_5 voltage regulator internal resistors are used (IRS = “H”).	2

System Bus Connection Terminals

Pin Name	I/O	Function	No. of Pins
D7 to D0 (SI) (SCL)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). At this time, D0 to D5 are set to high impedance. When the chip select is inactive, D0 to D7 are set to high impedance.	8
A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.	1
$\overline{RES}$	I	When $\overline{RES}$ is set to "L," the settings are initialized. The reset operation is performed by the $\overline{RES}$ signal level.	1
$\overline{CS1}$ CS2	I	This is the chip select signal. When $\overline{CS1}$ = "L" and CS2 = "H," then the chip select becomes active, and data/command I/O is enabled.	2
$\overline{RD}$ (E)	I	• When connected to an 8080 MPU, this is active LOW. This pin is connected to the $\overline{RD}$ signal of the 8080 MPU, and the SED1565 series data bus is in an output status when this signal is "L". • When connected to a 6800 Series MPU, this is active HIGH. This is the 68000 Series MPU enable clock input terminal.	1
$\overline{WR}$ (R/$\overline{W}$)	I	• When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/$\overline{W}$ = "H": Read. When R/$\overline{W}$ = "L": Write.	1
C86	I	This is the MPU interface switch terminal. C86 = "H": 6800 Series MPU interface. C86 = "L": 8080 MPU interface.	1
P/S	I	This is the parallel data input/serial data input switch terminal. P/S = "H": Parallel data input. P/S = "L": Serial data input. The following applies depending on the P/S status: **P/S** | **Data/Command** | **Data** | **Read/Write** | **Serial Clock** "H" | A0 | D0 to D7 | $\overline{RD}$, $\overline{WR}$ | "L" | A0 | SI (D7) | Write only | SCL (D6) When P/S = "L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or Open. $\overline{RD}$ (E) and $\overline{WR}$ (P/$\overline{W}$) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.	1

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Terminal to select whether or enable or disable the display clock internal oscillator circuit.
CLS = “H”: Internal oscillator circuit is enabled
CLS = “L”: Internal oscillator circuit is disabled (requires external input)
When CLS = “L”, input the display clock through the CL terminal.</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the SED1565 Series chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.
M/S = “H”: Master operation
M/S = “L”: Slave operation
The following is true depending on the M/S and CLS status:
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>FRS</th><th>DOF</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td><td>Output
Output</td><td>Output
Output</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td><td>Output
Output</td><td>Input
Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>This is the display clock input terminal
The following is true depending on the M/S and CLS status.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>“H”</td><td>“H”
“L”</td><td>Output
Input</td></tr>
<tr><td>“L”</td><td>“H”
“L”</td><td>Input
Input</td></tr>
</table>
When the SED1565 Series chips are used in master/slave mode, the various CL terminals must be connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various FR terminals must be connected.</td><td>1</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = “H”: Output
M/S = “L”: Input
When the SED1565 Series chip is used in master/slave mode, the various $\overline{\text{DOF}}$ terminals must be connected.</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>This is the output terminal for the static drive.
This terminal is only enabled when the static indicator display is ON when in master operation mode, and is used in conjunction with the FR terminal.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This terminal selects the resistors for the V5 voltage level adjustment.
IRS = “H”: Use the internal resistors
IRS = “L”: Do not use the internal resistors. The V5 voltage level is regulated by an external resistive voltage divider attached to the VR terminal.
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
<tr><td>$\overline{\text{HPM}}$</td><td>I</td><td>This is the power control terminal for the power supply circuit for liquid crystal drive.
$\overline{\text{HPM}}$ = “H”: Normal mode
$\overline{\text{HPM}}$ = “L”: High power mode
This pin is enabled only when the master operation mode is selected.
It is fixed to either “H” or “L” when the slave operation mode is selected.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Terminals

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>No. of Pins</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>These are the liquid crystal segment drive outputs. Through a combination of the contents of the display RAM and with the FR signal, a single level is selected from V_{DD}, V_2, V_3, and V_5.
<table>
<tr><th>RAM DATA</th><th>FR</th><th colspan="2">Output Voltage</th></tr>
<tr><td></td><td></td><td>Normal Display</td><td>Reverse Display</td></tr>
<tr><td>H</td><td>H</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_5</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0
to
COMn</td><td>O</td><td>These are the liquid crystal common drive outputs.
<table>
<tr><th>Part No.</th><th>COM</th></tr>
<tr><td>SED1565*** </td><td>COM 0 ~ COM 63</td></tr>
<tr><td>SED1566*** </td><td>COM 0 ~ COM 47</td></tr>
<tr><td>SED1567*** </td><td>COM 0 ~ COM 31</td></tr>
<tr><td>SED1568*** </td><td>COM 0 ~ COM 53</td></tr>
<tr><td>SED1569*** </td><td>COM 0 ~ COM 51</td></tr>
</table>
<table>
<tr><th>Part No.</th><th></th></tr>
<tr><td>SED1565*** </td><td>64</td></tr>
<tr><td>SED1566*** </td><td>48</td></tr>
<tr><td>SED1567*** </td><td>32</td></tr>
<tr><td>SED1568*** </td><td>54</td></tr>
<tr><td>SED1569*** </td><td>52</td></tr>
</table>
Through a combination of the contents of the scan data and with the FR signal, a single level is selected from V_{DD}, V_1, V_4, and V_5.
<table>
<tr><th>Scan Data</th><th>FR</th><th>Output Voltage</th></tr>
<tr><td>H</td><td>H</td><td>V_5</td></tr>
<tr><td>H</td><td>L</td><td>V_{DD}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
<tr><td>Power Save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td></td></tr>
<tr><td>COMS</td><td>O</td><td>These are the COM output terminals for the indicator. Both terminals output the same signal.
Leave these open if they are not used.
When in master/slave mode, the same signal is output by both master and slave.</td><td>2</td></tr>
</table>

Test Terminals

Pin Name	I/O	Function	No. of Pins
TEST0 to 4 TEST7 to 9	I/O	These are terminals for IC chip testing. They are set to OPEN.	12
TEST5, 6	I	These are terminals for IC chip testing. They are set to V_{DD}.	2

Total: 288 pins for the SED1565***.
272 pins for the SED1566***.
256 pins for the SED1567***.

DESCRIPTION OF FUNCTIONS

The MPU Interface

Selecting the Interface Type

With the SED1565 Series chips, data transfers are done through an 8-bit bi-directional data bus (D7 to D0) or through a serial data input (SI). Through selecting the P/S terminal polarity to the "H" or "L" it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
H: Parallel Input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5~D0
L: Serial Input	CS1	CS2	A0	—	—	—	SI	SCL	(HZ)

"—" indicates fixed to either "H" or to "L"

The Parallel Interface

When the parallel interface has been selected (P/S = "H"), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (as shown in Table 2) by selecting the C86 terminal to either "H" or to "L".

Table 2

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0
H: 6800 Series MPU Bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7~D0
L: 8080 MPU Bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7~D0

Moreover, data bus signals are recognized by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

The Serial Interface

When the serial interface has been selected (P/S = "L") then when the chip is in active state ($\overline{CS1}$ = "L" and CS2 = "H") the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits parallel data in the rising edge of the eighth serial clock for the processing.
The A0 input is used to determine whether or the serial data input is display data or command data; when A0 = "H", the data is display data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.
Figure 1 is a serial interface signal chart.

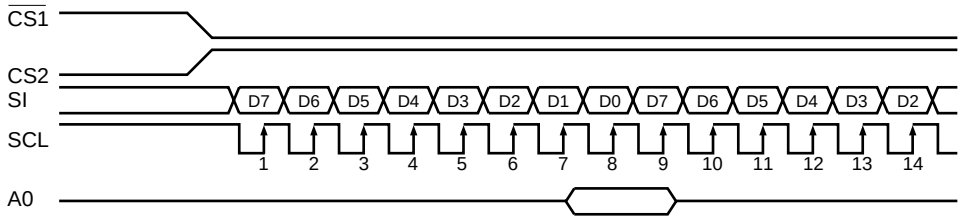


Figure 1

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

The Chip Select

The SED1565 Series chips have two chip select terminals: $\overline{CS1}$ and CS2. The MPU interface or the serial interface is enabled only when $\overline{CS1}$ = "L" and CS2 = "H".
When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, $\overline{RD}$, and $\overline{WR}$ inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

Accessing the Display Data RAM and the Internal Registers

Data transfer at a higher speed is ensured since the MPU is required to satisfy the cycle time (t_{CYC}) requirement alone in accessing the SED1565 Series. Wait time may not be considered.
And, in the SED1565 Series chips, each time data is sent from the MPU, a type of pipeline process between LSIs is performed through the bus holder attached to the internal data bus.
For example, when the MPU writes data to the display data RAM, once the data is stored in the bus holder, then it is written to the display data RAM before the next data write cycle. Moreover, when the MPU reads the display data RAM, the first data read cycle (dummy) stores the read data in the bus holder, and then the data is read from the bus holder to the system bus at the next data read cycle.
There is a certain restriction in the read sequence of the display data RAM. Please be advised that data of the specified address is not generated by the read instruction issued immediately after the address setup. This data is generated in data read of the second time. Thus, a dummy read is required whenever the address setup or write cycle operation is conducted.
This relationship is shown in Figure 2.

The Busy Flag

When the busy flag is "1" it indicates that the SED1565 Series chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pin with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

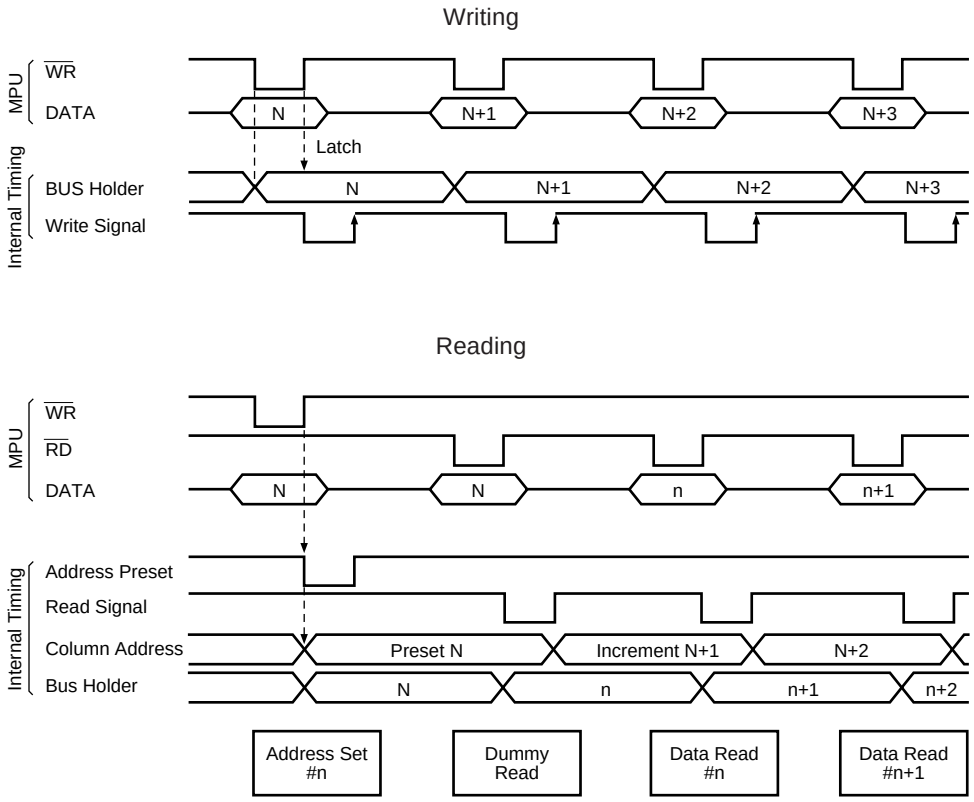


Figure 2

Display Data RAM

Display Data RAM

The display data RAM is a RAM that stores the dot data for the display. It has a 65 (8 page x 8 bit +1) x 132 bit structure. It is possible to access the desired bit by specifying the page address and the column address.
Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display data transfer when multiple SED1565 series chips are used, thus and display structures can be created easily and with a high degree of freedom.
Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, it will not cause adverse effects on the display (such as flickering).

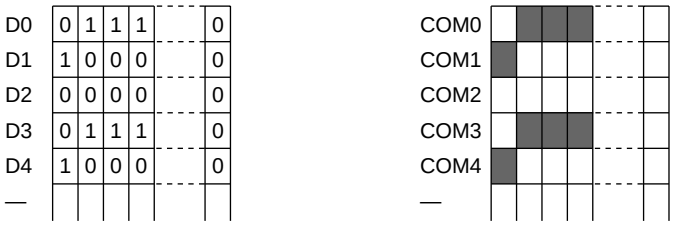


Figure 3

The Page Address Circuit

As shown in Figure 6-4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.
Page address 8 (D3, D2, D1, D0 = 1, 0, 0, 0) is the page for the RAM region used only by the indicators, and only display data D0 is used.

The Column Addresses

As is shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously. Moreover, the incrementation of column addresses stops with 83H. Because the column address is independent of the page address, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to respecify both the page address and the column address.
Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG 131
ADC "0"	0 (H) →	Column Address	→ 83 (H)
(D0) "1"	83 (H) ←	Column Address	← 0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified (this is the COM0 output when the common output mode is normal, and the COM63 output for SED1565 Series, COM47 output for SED1566 Series and COM31 output for the SED1567 Series when the common output mode is reversed. The display area is a 65 line area for the SED1565 Series, a 49 line are for the SED1566 and a 33 line area for the SED1567 Series from the display start line address.
If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

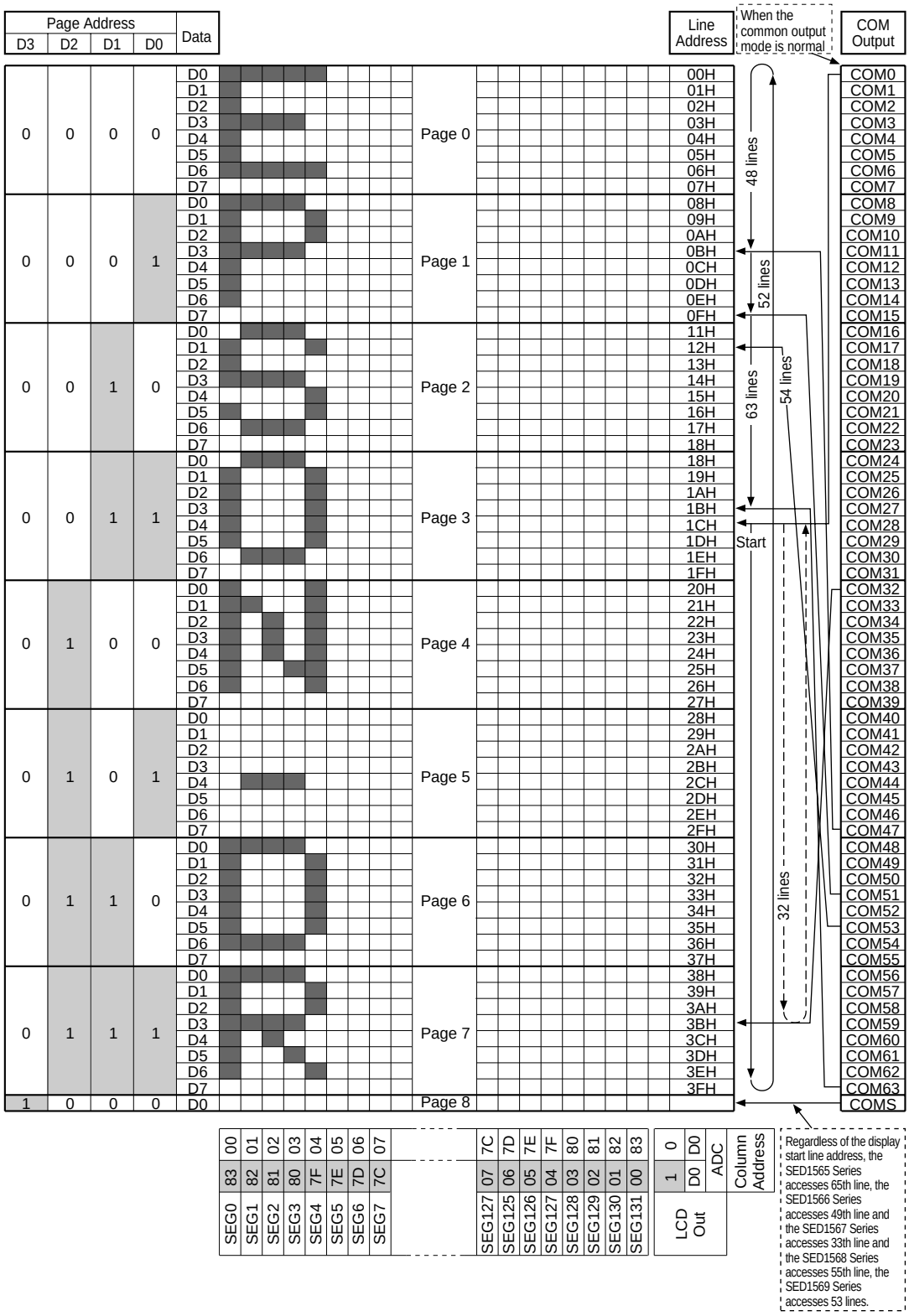

Page Address
D3
D2
D1
D0
Data
Line Address
When the common output mode is normal
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
48 lines
52 lines
63 lines
54 lines
32 lines
Start
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
COM16
COM17
COM18
COM19
COM20
COM21
COM22
COM23
COM24
COM25
COM26
COM27
COM28
COM29
COM30
COM31
COM32
COM33
COM34
COM35
COM36
COM37
COM38
COM39
COM40
COM41
COM42
COM43
COM44
COM45
COM46
COM47
COM48
COM49
COM50
COM51
COM52
COM53
COM54
COM55
COM56
COM57
COM58
COM59
COM60
COM61
COM62
COM63
COMS
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG127
SEG125
SEG126
SEG127
SEG128
SEG129
SEG130
SEG131
LCD Out
Column Address
ADC
Regardless of the display start line address, the SED1565 Series accesses 65th line, the SED1566 Series accesses 49th line and the SED1567 Series accesses 33th line and the SED1568 Series accesses 55th line, the SED1569 Series accesses 53 lines.

Figure 4

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.
Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H".
When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of accesses to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.
Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive wave form using a 2 frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

Two-frame alternating current drive wave form (SED1565***)

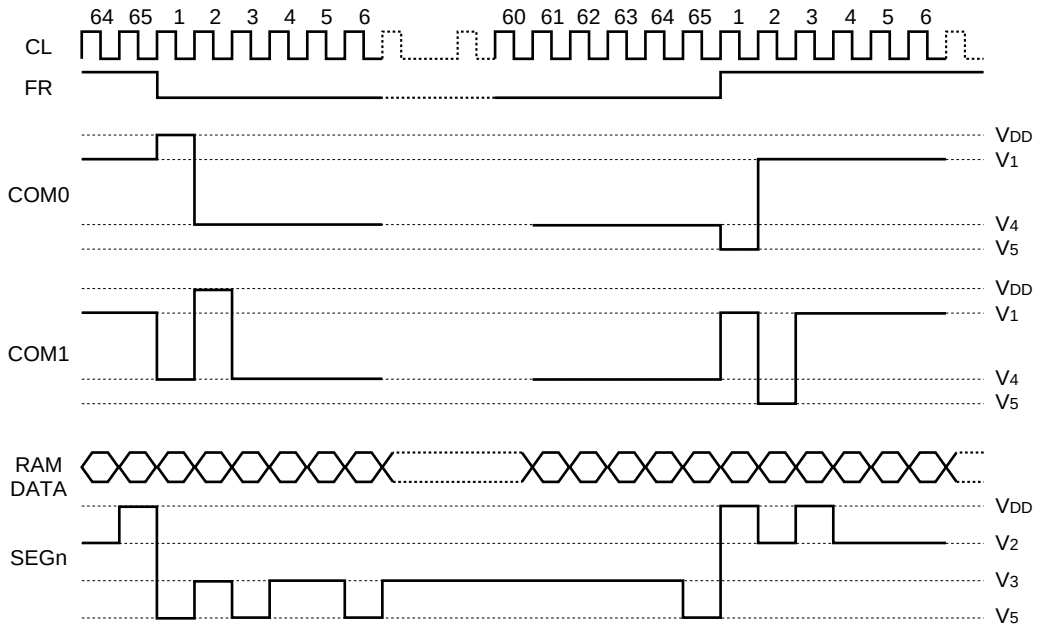


Figure 5

When multiple SED1565 Series chips are used, the slave chips must be supplied the display timing signals (FR, CL, $\overline{DOF}$) from the master chip[s].
Table 5 shows the status of the FR, CL, and $\overline{DOF}$ signals.

Table 5

Operating Mode		FR	CL	$\overline{DOF}$
Master (M/S = "H")	The internal oscillator circuit is enabled (CLS = "H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal oscillator circuit is enabled (CLS = "H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS = "L")	Input	Input	Input

The Common Output Status Select Circuit

In the SED1565 Series chips, the COM output scan direction can be selected by the common output status select command. (See Table 6.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Table 6

Status	COM Scan Direction				
	SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
Normal	COM0 → COM63	COM0 → COM47	COM0 → COM31	COM0 → COM53	COM0 → COM51
Reverse	COM63 → COM0	COM47 → COM0	COM31 → COM0	COM53 → COM0	COM51 → COM0

The Liquid Crystal Driver Circuits

These are a 197-channel (SED1565 Series), a 181-channel (SED1566 Series) multiplexers 165-channel (SED1567 Series) and a 185-channel (SED1569 Series) that generate four voltage levels for driving the liquid crystal. The combination of the display data, the COM scan signal, and the FR signal produces the liquid crystal drive voltage output.
Figure 6 shows examples of the SEG and COM output wave form.

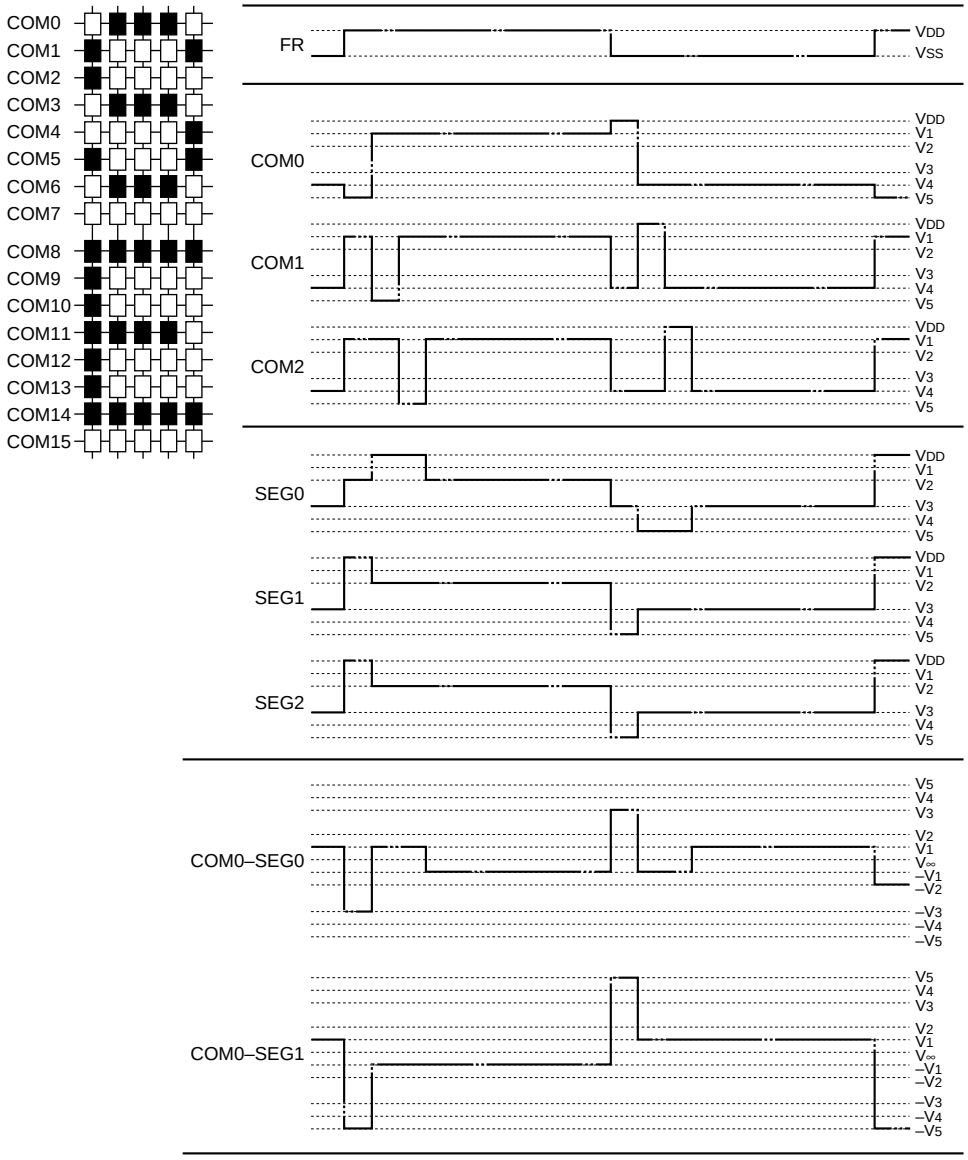

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
V1
V2
V3
V4
V5
SEG0
SEG1
SEG2
COM0–SEG0
COM0–SEG1
V∞
–V1
–V2
–V3
–V4
–V5

Figure 6

The Power Supply Circuits

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON of OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 7 shows the Power Control Set Command 3-bit data control function, and Table 8 shows reference combinations.

Table 7 The Control Details of Each Bit of the Power Control Set Command

Item	Status "1"	Status "0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit) control bit	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference Combinations

Use Settings	D2	D1	D0	Step-up circuit	V regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
① Only the internal power supply is used	1	1	1	O	O	O	V_{SS2}	Used
② Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V_{OUT}, V_{SS2}	Open
③ Only the V/F circuit is used	0	0	1	X	X	O	V_5, V_{SS2}	Open
④ Only the external power supply is used	0	0	0	X	X	X	V_1 to V_5	Open

* The "step-up system terminals" refer CAP1+, CAP1–, CAP2+, CAP2–, and CAP3–.

* While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits equipped within the SED1565 Series chips it is possible to product a Quad step-up, a Triple step-up, and a Double step-up of the $V_{DD} - V_{SS2}$ voltage levels.

Quad step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2–, between CAP1+ and CAP3–, and between V_{SS2} and V_{OUT}, to produce a voltage level in the negative direction at the V_{OUT} terminal that is 4 times the voltage level between V_{DD} and V_{SS2}.

Triple step-up: Connect capacitor C1 between CAP1+ and CAP1–, between CAP2+ and CAP2– and between V_{SS2} and V_{OUT}, and short between CAP3– and V_{OUT} to produce a voltage level in the negative direction at the V_{OUT} terminal that is 3 times the voltage difference between V_{DD} and V_{SS2}.

Double step-up: Connect capacitor C1 between CAP1+ and CAP1–, and between V_{SS2} and V_{OUT}, leave CAP2+ open, and short between CAP2–, CAP3– and V_{OUT} to produce a voltage in the negative direction at the V_{OUT} terminal that is twice the voltage between V_{DD} and V_{SS2}.

The step-up voltage relationships are shown in Figure 7.

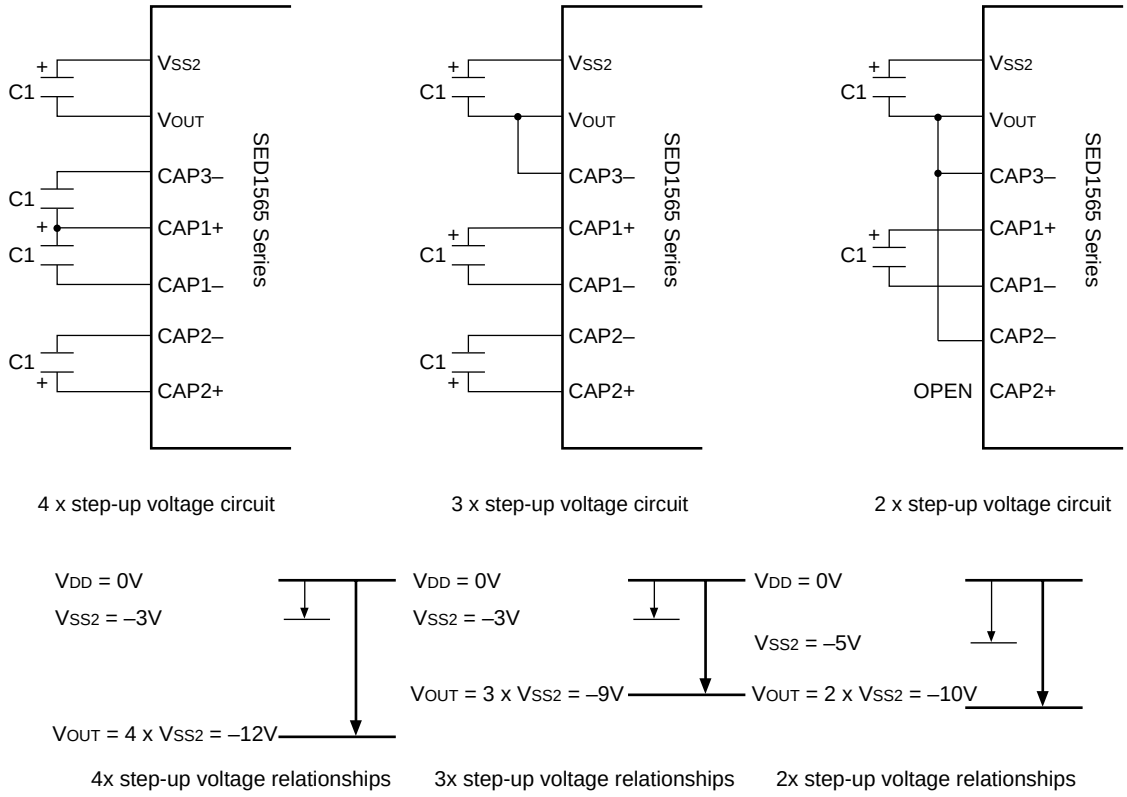


Figure 7

* The V_{SS2} voltage range must be set so that the V_{OUT} terminal voltage does not exceed the absolute maximum rated value.

The Voltage Regulator Circuit

The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_5 through the voltage regulator circuit.

Because the SED1565 Series chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_5 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, in the SED1565 Series, three types of thermal gradients have been prepared as V_{REG} options: (1) approximately -0.05%/°C (2) approximately -0.2%/°C, and (3) external input (supplied to the V_{RS} terminal).

(A) When the V_5 Voltage Regulator Internal Resistors Are Used

Through the use of the V_5 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V_5 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V_5 voltage can be calculated using equation A-1 over the range where $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1 + \frac{Rb}{Ra}\right) \cdot V_{EV}$$
$$= \left(1 + \frac{Rb}{Ra}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation A-1)}$$

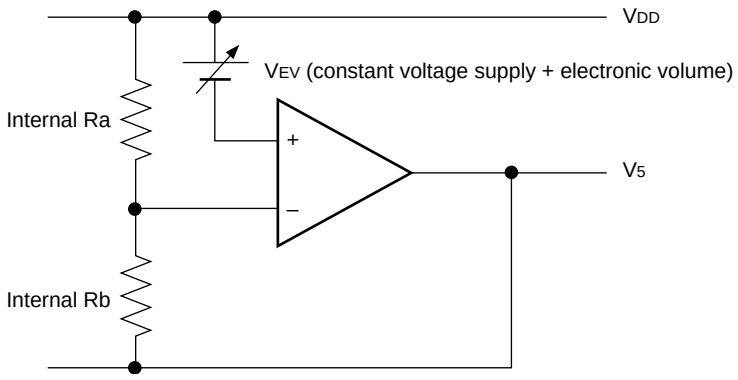


Figure 8

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 9.

Table 9

Equipment Type	Thermal Gradient	Units	VREG	Units
(1) Internal Power Supply	–0.05	[%/°C]	–2.1	[V]
(2) Internal Power Supply	–0.2	[%/°C]	–4.9	[V]
(3) External Input	—	—	VRS	[V]

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
		⋮				⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra is the V5 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V5 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V5 voltage regulator internal resistor ratio register.

V_5 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 11

Register			SED1565***			SED1566***		
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]		
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	(1) –0.05	(2) –0.2	(3) V_{REG} External Input
0	0	0	3.0	1.3	1.5	3.0	1.3	1.5
0	0	1	3.5	1.5	2.0	3.5	1.5	2.0
0	1	0	4.0	1.8	2.5	4.0	1.8	2.5
0	1	1	4.5	2.0	3.0	4.5	2.0	3.0
1	0	0	5.0	2.3	3.5	5.0	2.3	3.5
1	0	1	5.5	2.5	4.0	5.4	2.5	4.0
1	1	0	6.0	2.8	4.5	5.9	2.8	4.5
1	1	1	6.4	3.0	5.0	6.4	3.0	5.0

Register			SED1567***			SED1568***/SED1569***
			Equipment Type by Thermal Gradient [Units: %/°C]			Equipment Type by Thermal Gradient [Units: %/°C]
D2	D1	D0	(1) –0.05	(2) –0.2	(3) V_{REG} External Input	–0.05
0	0	0	3.0	1.3	1.5	3
0	0	1	3.5	1.5	2.0	3.5
0	1	0	4.0	1.8	2.5	4
0	1	1	4.5	2.0	3.0	4.5
1	0	0	5.0	2.3	3.5	5
1	0	1	5.4	2.5	4.0	5.4
1	1	0	5.9	2.8	4.5	5.9
1	1	1	6.4	3.0	5.0	6.4

Figs. 9, 10, 11 (for SED1565 Series), 12, 13, 14 (for SED1566 Series) and Figs. 15, 16, 17 show V_5 voltage measured by values of the internal resistance ratio resistor for V_5 voltage adjustment and electric volume resister for each temperature grade model, when Ta = 25 °C.

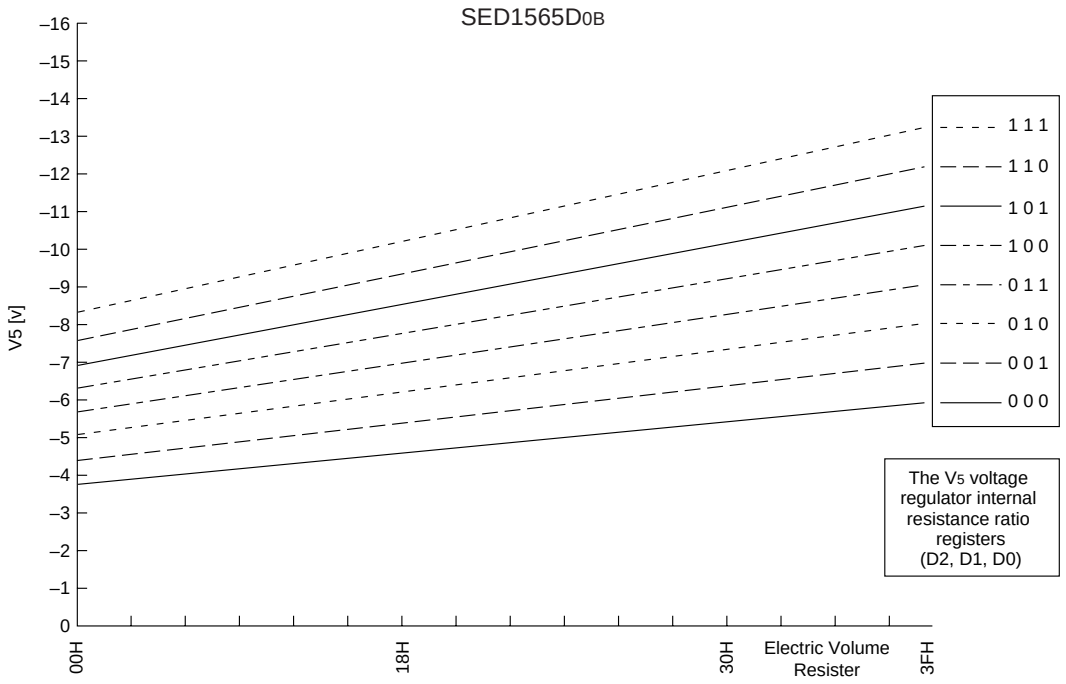


Figure 9: SED1565D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

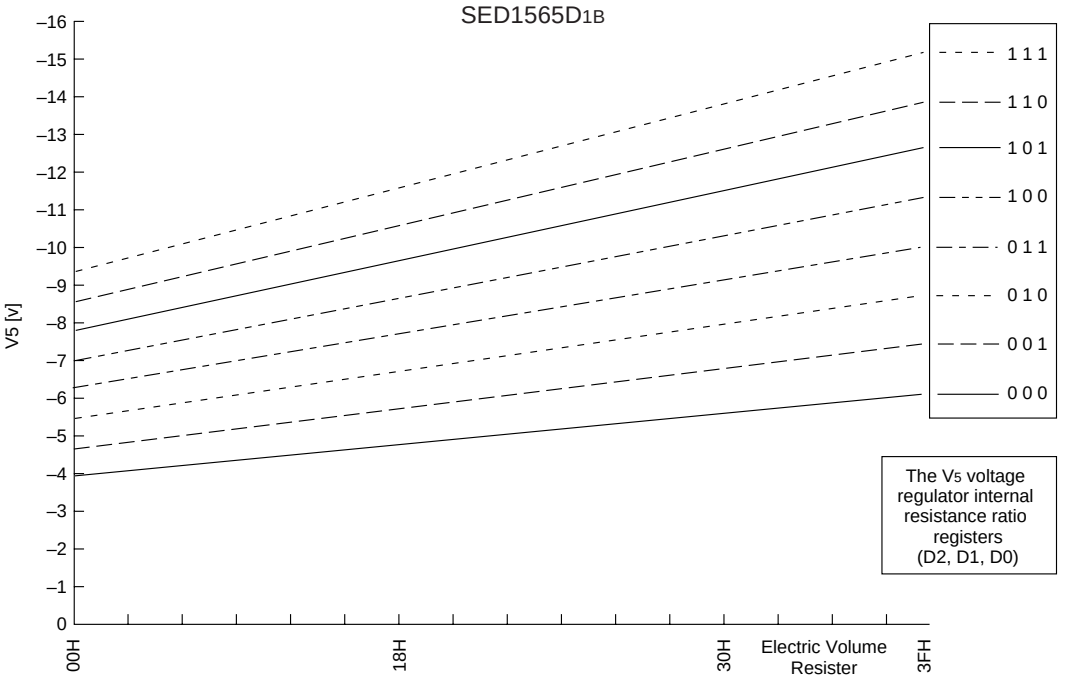


Figure 10: SED1565D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

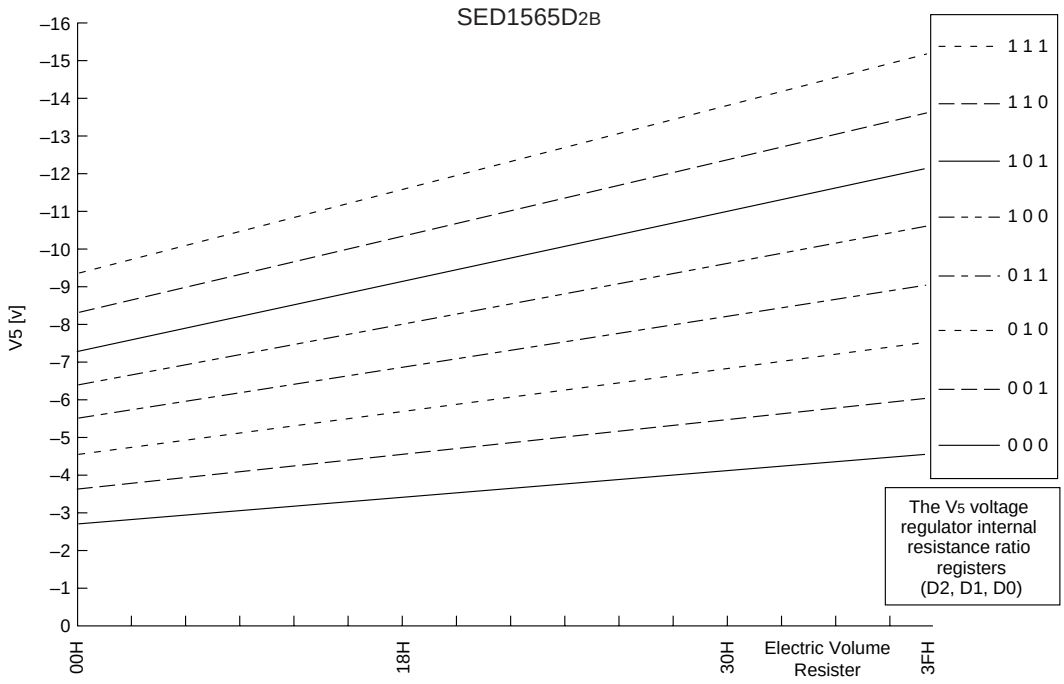


Figure 11: SED1565D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

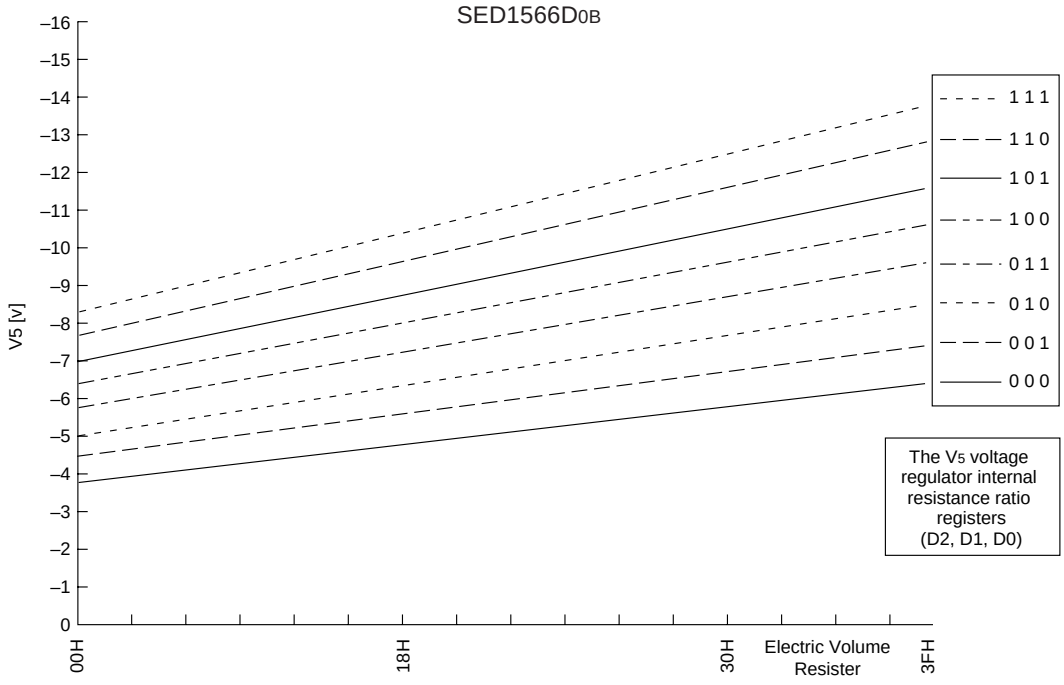


Figure 12: SED1566D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

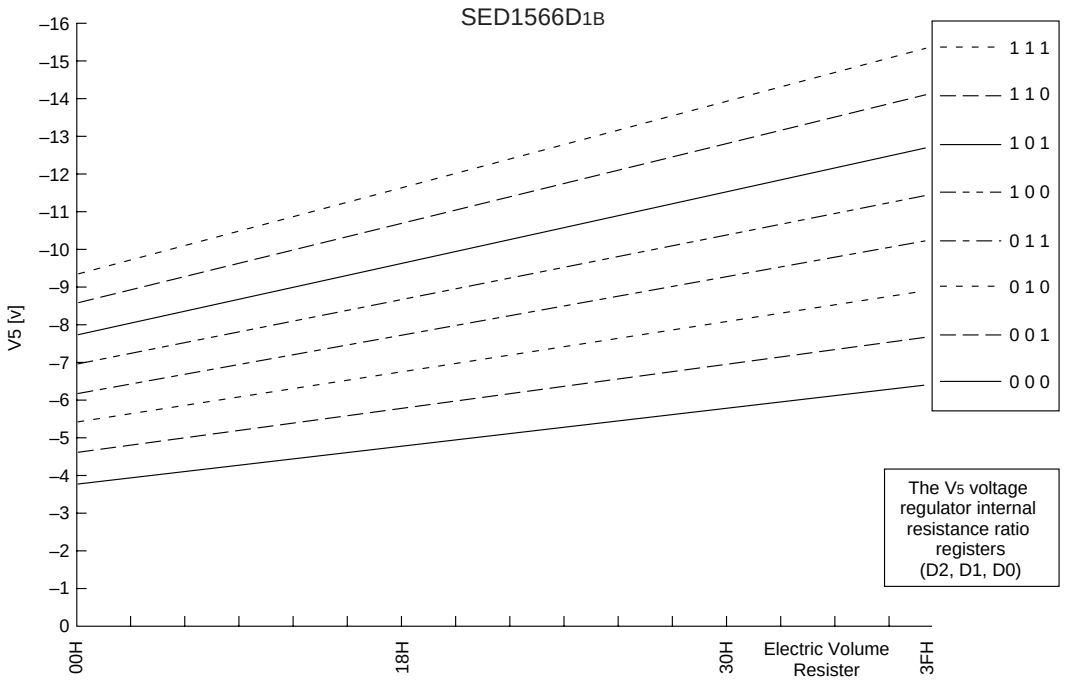


Figure 13: SED1566D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

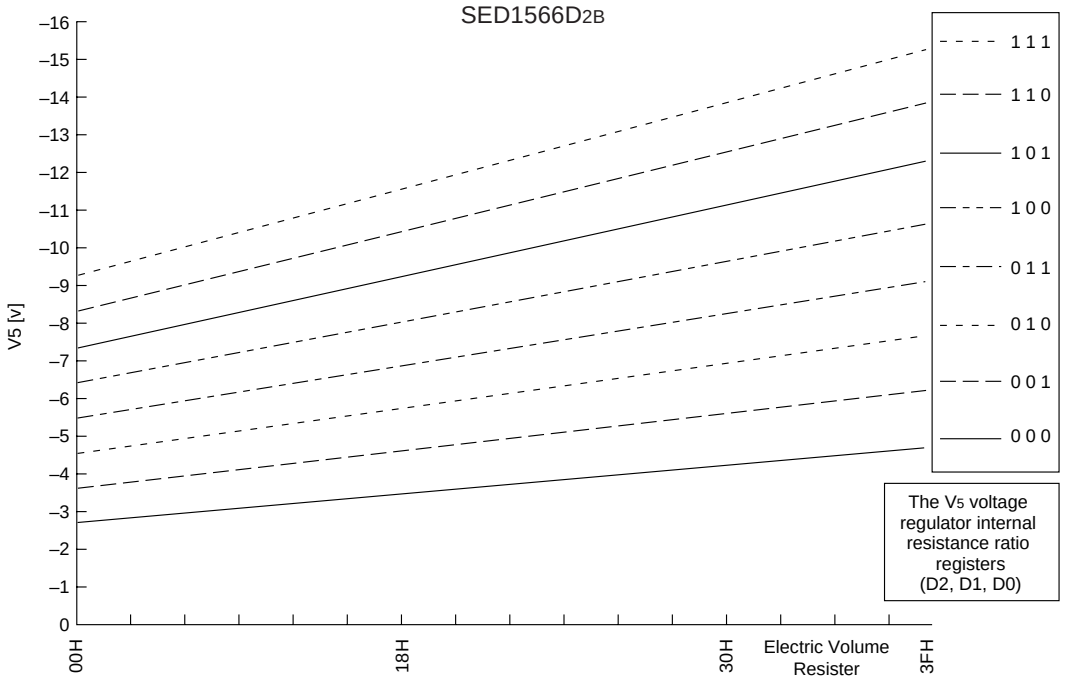


Figure 14: SED1566D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

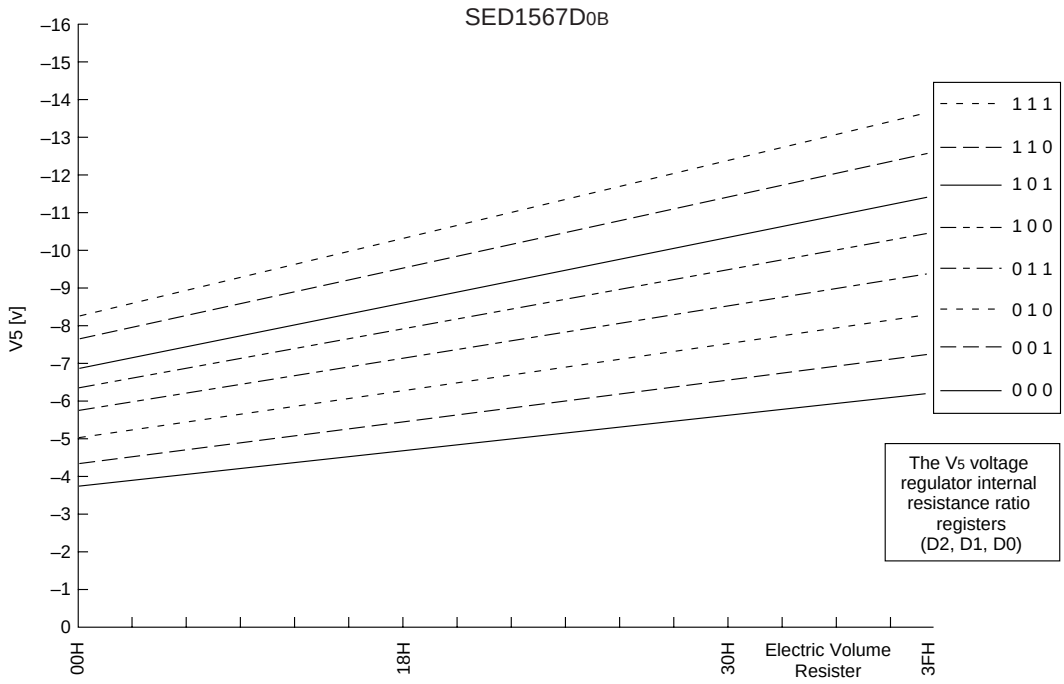


Figure 15: SED1567D0B (1) For Models Where the Thermal Gradient = -0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

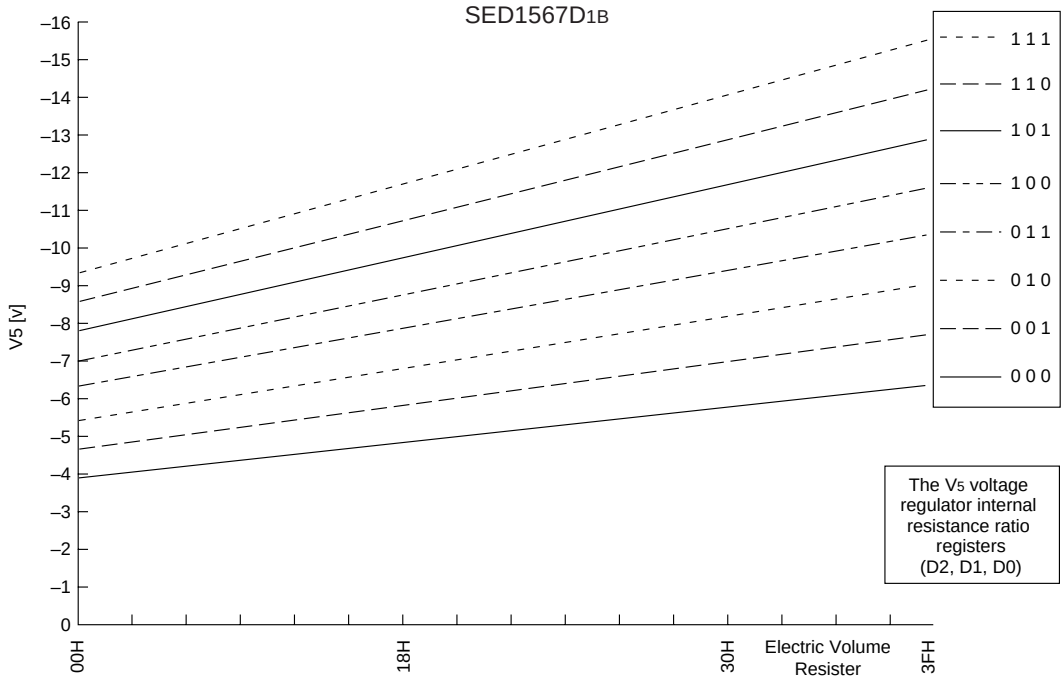


Figure 16: SED1567D1B (2) For Models Where the Thermal Gradient = -0.2%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

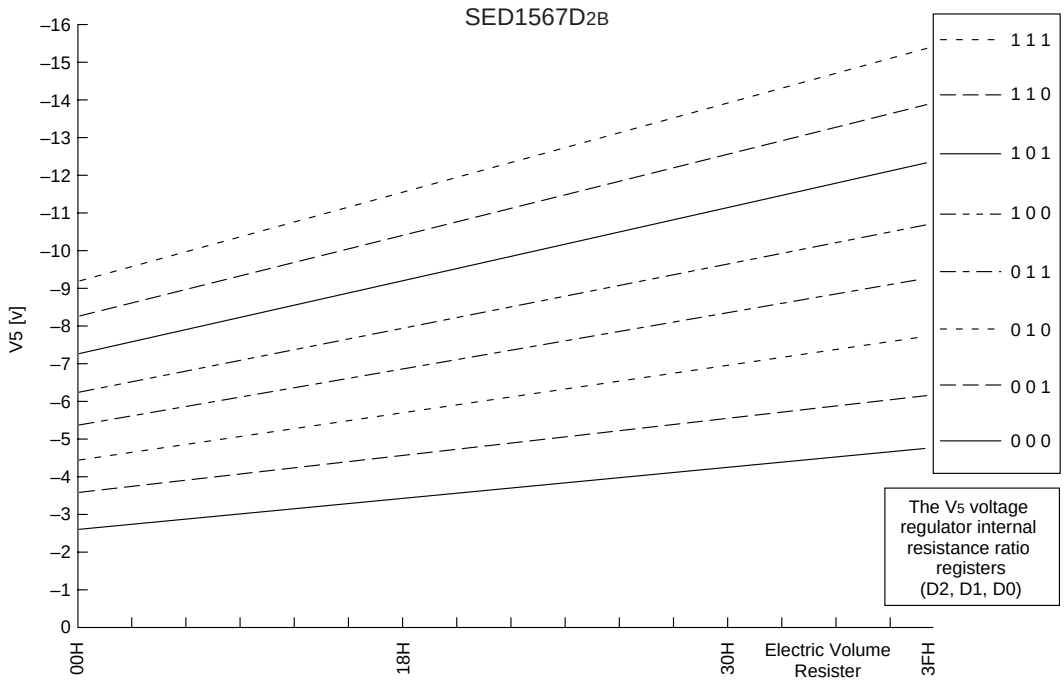


Figure 17: SED1567D2B (3) For models with External Input

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

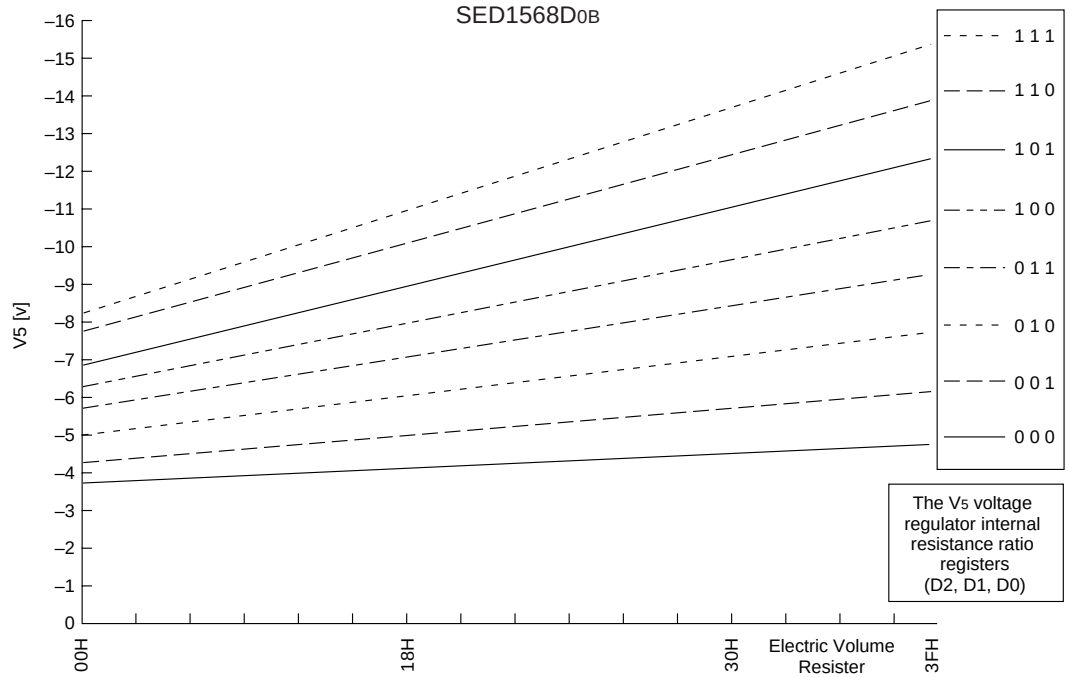


Figure 18: SED1568D0B (1) For Models Where the Thermal Gradient = –0.05%/°C

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

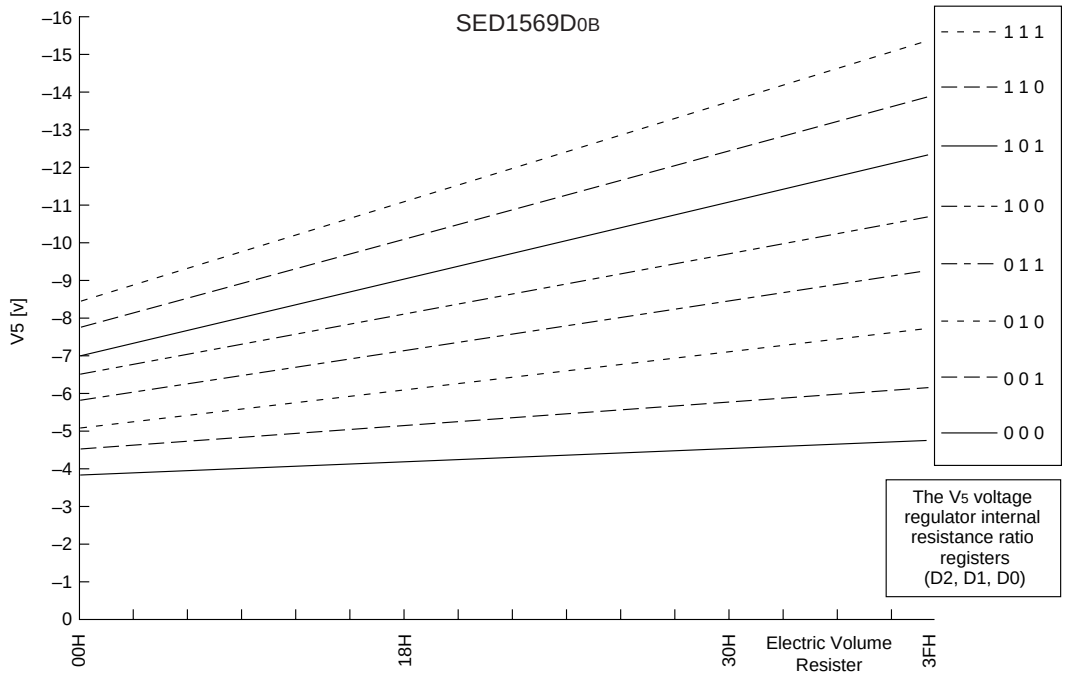


Figure 19: SED1569D0B (Temperature Gradient = –0.05%/°C Model

The V_5 voltage as a function of the V_5 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example: When selecting Ta = 25°C and V_5 = 7 V for an SED1567 model on which Temperature gradient = –0.05%/°C.
Using Figure 15 and the equation A-1, the following setup is enabled.

Table 12

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V_5 voltage regulator	—	—	—	0	1	0
Electronic Volume	1	0	0	1	0	1

At this time, the variable range and the notch width of the V_5 voltage is, as shown Table 13, as dependent on the electronic volume.

Table 13

V_5	Min	Typ	Max	Units
Variable Range	–8.4 (63 levels)	–6.8 (central value)	–5.1 (0 level)	[V]
Notch width		51		[mV]

(B) When an External Resistance is Used (i.e., The V5 Voltage Regulator Internal Resistors Are Not Used) (1)

The liquid crystal power supply voltage V5 can also be set without using the V5 voltage regulator internal resistors (IRS terminal = "L") by adding resistors Ra' and Rb' between VDD and VR, and between VR and V5, respectively. When this is done, the use of the electronic volume function makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal power supply voltage V5 through commands. In the range where | V5 | < | VOUT |, the V5 voltage can be calculated using equation B-1 based on the external resistances Ra' and Rb'.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV}$$
$$= \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$\left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Equation B-1)}$$

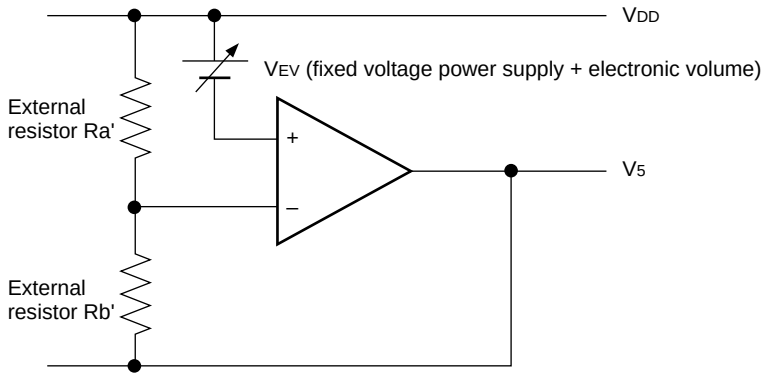


Figure 20

Setup example: When selecting Ta = 25°C and V5 = –7 V for an SED1567 Series model where the temperature gradient = –0.05%/°C.
When the central value of the electron volume register is (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0), then α = 31 and VREG = –2.1 V so, according to equation B-1,

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG}$$
$$-11V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1) \qquad \text{(Equation B-2)}$$

Moreover, when the value of the current running through Ra' and Rb' is set to 5 μA,

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Equation B-3)}$$

Consequently, by equations B-2 and B-3,

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

At this time, the V5 voltage variable range and notch width, based on the electron volume function, is as given in Table 14.

Table 14

V5	Min	Typ	Max	Units
Variable Range	–8.6 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		52		[mV]

(C) When External Resistors are Used (i.e. The V_5 Voltage Regulator Internal Resistors Are Not Used). (2)

When the external resistor described above are used, adding a variable resistor as well makes it possible to perform fine adjustments on Ra' and Rb', to set the liquid crystal drive voltage V_5. In this case, the use of the electronic volume function makes it possible to control the liquid crystal power supply voltage V_5 by commands to adjust the liquid crystal display brightness. In the range where $|V_5| < |V_{OUT}|$ the V_5 voltage can be calculated by equation C-1 below based on the R_1 and R_2 (variable resistor) and R_3 settings, where R_2 can be subjected to fine adjustments (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \qquad \text{(Equation C-1)}$$

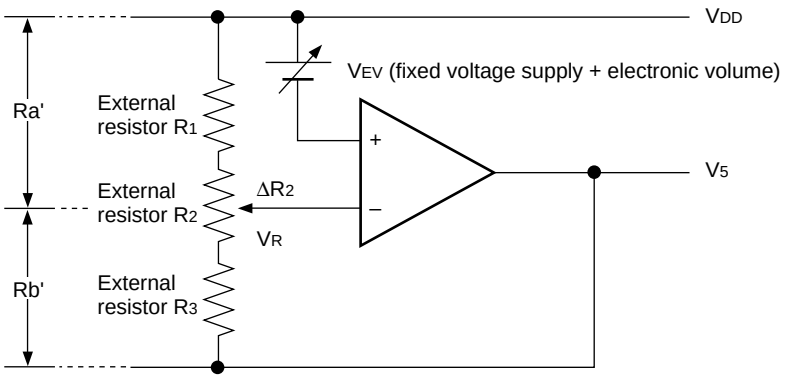


Figure 21

Setup example: When selecting Ta = 25°C and V_5 = –5 to –9 V (using R2) for an SED1567 model where the temperature gradient = –0.05%/°C.
When the central value for the electronic volume register is set at (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0),

$$\alpha = 31$$

$$V_{REG} = -2.1V$$

so, according to equation C-1, when $\Delta R_2 = 0\ \Omega$, in order to make V_5 = –9 V,

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-2)

When $\Delta R_2 = R_2$, in order to make V = –5 V,

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Equation C-3)

Moreover, when the current flowing V_{DD} and V_5 is set to 5 µA,

$$R_1 + R_2 + R_3 = 1.4M\Omega \qquad \text{(Equation C-4)}$$

With this, according to equation C-2, C-3 and C-4,

$$R_1 = 264k\Omega$$

$$R_2 = 211k\Omega$$

$$R_3 = 925k\Omega$$

At this time, the V_5 voltage variable range and notch width based on the electron volume function is as shown in Table 15.

Table 15

V_5	Min	Typ	Max	Units
Variable Range	–8.7 (63 levels)	–7.0 (central value)	–5.3 (0 level)	[V]
Notch width		53		[mV]

* When the V_5 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{OUT} when the Booster circuit is OFF.
* The V_R terminal is enabled only when the V_5 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V_5 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the V_R terminal is left open.
* Because the input impedance of the V_R terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V_5 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V_1, V_2, V_3, and V_4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V_1, V_2, V_3 and V_4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for SED1565 Series, 1/8 bias or 1/6 bias for SED1566 Series and 1/6 bias or 1/5 bias for the SED1567 Series can be selected.

High Power Mode

The power supply circuit equipped in the SED1565 Series chips has very low power consumption (normal mode: $\overline{HPM}$ = "H"). However, for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the $\overline{HPM}$ terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.
Moreover, if the improvement to the display is inadequate even after high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

The Internal Power Supply Shutdown Command Sequence

The sequence shown in Figure 20 is recommended for shutting down the internal power supply, first placing the power supply in power saver mode and then turning the power supply OFF.

Sequence	Details (Command, status)	Command address D7	D6	D5	D4	D3	D2	D1	D0	
Step1	Display OFF	1	0	1	0	1	1	1	0	Power saver commands (compound)
↓										
Step2	Display all points ON	1	0	1	0	0	1	0	1	
↓										
End	Internal power supply OFF									

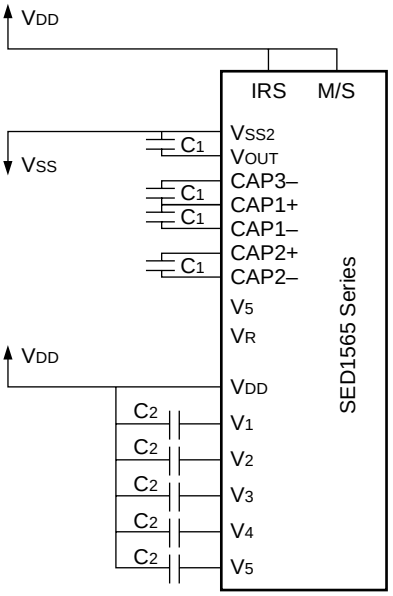
Figure 22

Reference Circuit Examples

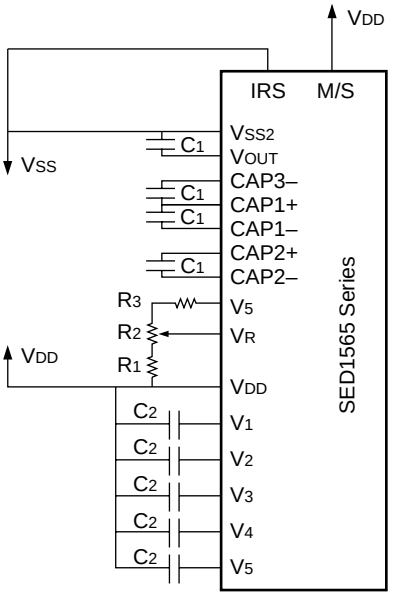
Figure 22 shows reference circuit examples.

① When used all of the step-up circuit, voltage regulating circuit and V/F circuit

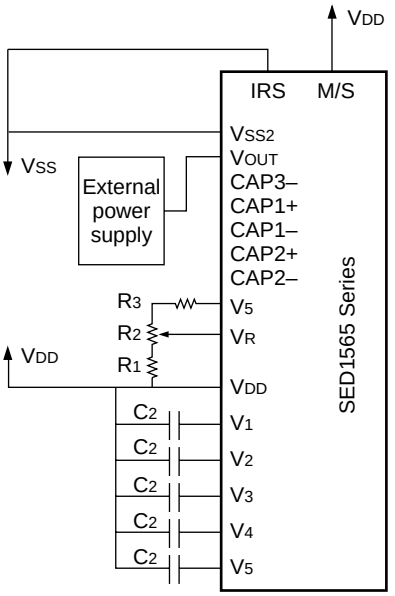
(1) When the voltage regulator internal resistor is used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)



(2) When the voltage regulator internal resistor is not used.
(Example where $V_{SS2} = V_{SS}$, with 4x step-up)

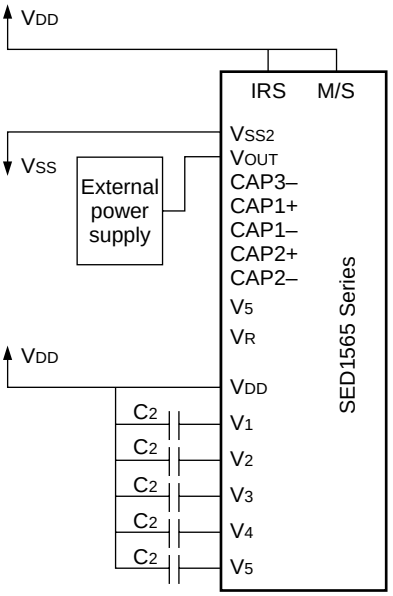


② When the voltage regulator circuit and V/F circuit alone are used
When the V_5 voltage regulator internal resistor is not used.

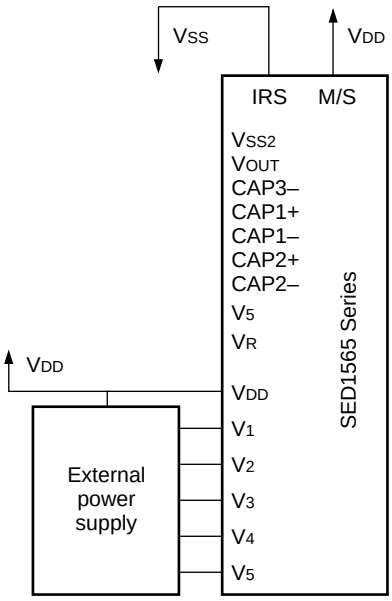


③ When the V/F circuit alone is used

When the V_5 voltage regulator internal resistor is used.



④ When the built-in power is not used



Examples of shared reference settings
When V_5 can vary between –8 and 12 V

Item	Set value	Units
C_1	1.0 ~ 4.7	µF
C_2	0.47 ~ 1.0	µF

Figure 23

* 1 Because the V_R terminal input impedance is high, use short leads and shielded lines.
* 2 C1 and C2 are determined by the size of the LCD being driven. Select a value that will stabilize the liquid crystal drive voltage.

Example of the Process by which to Determine the Settings:

- Turn the voltage regulator circuit and voltage follower circuit ON and supply a voltage to V_{OUT} from the outside.
- Determine C2 by displaying an LCD pattern with a heavy load (such as horizontal stripes) and selecting a C2 that stabilizes the liquid crystal drive voltages (V_1 to V_5). Note that all C2 capacitors must have the same capacitance value.
- Next turn all the power supplies ON and determine C1.

The Reset Circuit

When the $\overline{RES}$ input falls to "L", these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: normal (ADC command D0 = "L")
4. Power control register: (D2, D1, D0) = (0, 0, 0)
5. Serial interface internal register data clear
6. LCD power supply bias ratio:
   SED1565*** ..... 1/9 bias
   SED1566*** ..... 1/8 bias
   SED1567*** ..... 1/6 bias
7. Read modify write OFF
8. Stack indicator OFF
   Stack indicator register: (D1, D2) = (0, 0)
9. Display start line set to first line
10. Column address set to address 0
11. Page address set to page 0
12. Common output status normal
13. V_5 voltage regulator internal power supply ratio set mode clear
    V_5 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = "L").
17. Output condition of COM, SEG.
    COM : V1
    SEG : V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect.

As is described in "11. The MPU Interface (Reference Example)," the $\overline{RES}$ terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the $\overline{RES}$ terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition to the IC. After applying a current, it is necessary to take measures to prevent the input terminal from entering a high impedance state.

In the SED1565 Series, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply a "L" signal to the $\overline{RES}$ terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the $\overline{RES}$ terminal is "L," the display timing generator circuit is stopped, and the FR, FRS, and $\overline{DOF}$ terminals are fixed to "H" and the CL pin is fixed to "H" only when the internal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

COMMANDS

The SED1565 Series chips identify the data bus signals by a combination of A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only, and thus the processing is fast enough that normally a busy check is not required.
In the 8080 MPU interface, commands are launched by inputting a low pulse to the $\overline{RD}$ terminal for reading, and inputting a low pulse to the $\overline{WR}$ terminal for writing. In the 6800 Series MPU interface, the interface is placed in a read mode when an "H" signal is input to the R/$\overline{W}$ terminal and placed in a write mode when a "L" signal is input to the R/$\overline{W}$ terminal and then the command is launched by inputting a high pulse to the E terminal. (See "10. Timing Characteristics" regarding the timing.) Consequently, the 6800 Series MPU interface is different than the 80x86 Series MPU interface in that in the explanation of commands and the display commands the status read and display data read $\overline{RD}$ (E) becomes "1(H)". In the explanations below the commands are explained using the 8080 Series MPU interface as the example.
When the serial interface is selected, the data is input in sequence starting with D7.
<Explanation of Commands>

Display ON/OFF

This command turns the display ON and OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, power saver mode is entered. See the section on the power saver for details.

Display Start Line Set

This command is used to specify the display start line address of the display data RAM shown in Figure 4. For further details see the explanation of this function in "The Line Address Circuit".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

Page Address Set

This command specifies the page address corresponding to the low address when the MPU accesses the display data RAM (see Figure 4). Specifying the page address and column address enables to access a desired bit of the display data RAM. Changing the page address does not accompany a change in the status display. See the page address circuit in the Function Description (page 1–20) for the detail.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
									↓		↓
							0	1	1	1	7
							1	0	0	0	8

Column Address Set

This command specifies the column address of the display data RAM shown in Figure 4. The column address is split into two sections (the higher 4 bits and the lower 4 bits) when it is set (fundamentally, set continuously). Each time the display data RAM is accessed, the column address automatically increments (+1), making it possible for the MPU to continuously read from/write to the display data. The column address increment is topped at 83H. This does not change the page address continuously. See the function explanation in "The Column Address Circuit," for details.

	A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	A7	A6	A5	A4	A3	A2	A1	A0	Column address
High bits →	0	1	0	0	0	0	1	A7	A6	A5	A4	0	0	0	0	0	0	0	0	0
Low bits →							0	A3	A2	A1	A0	0	0	0	0	0	0	0	1	1
												0	0	0	0	0	0	1	0	2
																↓				↓
												1	0	0	0	0	0	1	0	130
												1	0	0	0	0	0	1	1	131

Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY = 1, it indicates that either processing is occurring internally or a reset condition is in process. While the chip does not accept commands until BUSY = 0, if the cycle time can be satisfied, there is no need to check for BUSY conditions.
ADC	This shows the relationship between the column address and the segment driver. 0: Reverse (column address 131-n ↔ SEG n) 1: Normal (column address n ↔ SEG n) (The ADC command switches the polarity.)
ON/OFF	ON/OFF: indicates the display ON/OFF state. 0: Display ON 1: Display OFF (This display ON/OFF command switches the polarity.)
RESET	This indicates that the chip is in the process of initialization either because of a $\overline{RES}$ signal or because of a reset command. 0: Operating state 1: Reset in progress

Display Data Write

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Display Data Read

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence between the display RAM data column address and the segment driver output. Thus, sequence of the segment driver output pins may be reversed by the command. See the column address circuit (page 1–20) for the detail. Increment of the column address (by "1") accompanying the reading or writing the display data is done according to the column address indicated in Figure 4.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

Display Normal/Reverse

This command can reverse the lit and unlit display without overwriting the contents of the display data RAM. When this is done the display data RAM contents are maintained.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM Data "H" LCD ON voltage (normal)
										1	RAM Data "L" LCD ON voltage (reverse)

Display All Points ON/OFF

This command makes it possible to force all display points ON regardless of the content of the display data RAM. The contents of the display data RAM are maintained when this is done. This command takes priority over the display normal/reverse command.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display mode
										1	Display all points ON

When the display is in an OFF mode, executing the display all points ON command will place the display in power save mode. For details, see the (20) Power Save section.

LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Select Status SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/8 bias	1/6 bias	1/8 bias	1/8 bias
										1	1/7 bias	1/6 bias	1/5 bias	1/6 bias	1/6 bias

Read/Modify/Write

This command is used paired with the "END" command. Once this command has been input, the display data read command does not change the column address, but only the display data write command increments (+1) the column address. This mode is maintained until the END command is input. When the END command is input, the column address returns to the address it was at when the read/modify/write command was entered. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as when there is a blanking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* Even in read/modify/write mode, other commands aside from display data read/write commands can also be used. However, the column address set command cannot be used.

• The sequence for cursor display

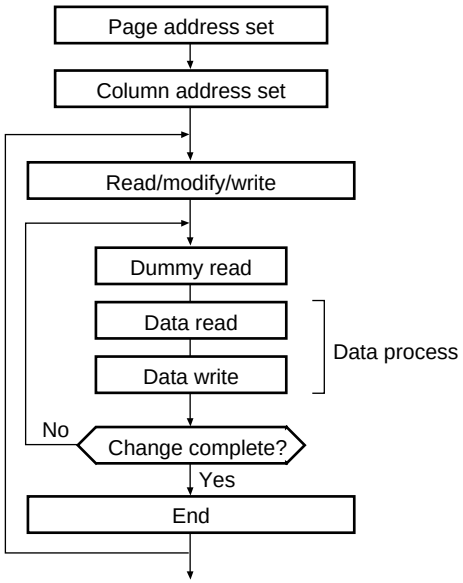


Figure 24

End

This command releases the read/modify/write mode, and returns the column address to the address it was at when the mode was entered.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

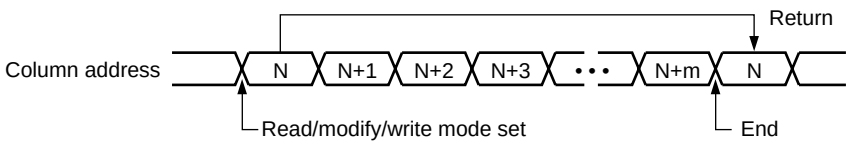


Figure 25

Reset

This command initializes the display start line, the column address, the page address, the common output mode, the V_5 voltage regulator internal resistor ratio, the electronic volume, and the static indicator are reset, and the read/modify/write mode and test mode are released. There is no impact on the display data RAM. See the function explanation in "Reset" for details.
The reset operation is performed after the reset command is entered.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power supply is applied must be done through applying a reset signal to the $\overline{RES}$ terminal. The reset command must not be used instead.

Common Output Mode Select

This command can select the scan direction of the COM output terminal. For details, see the function explanation in "Common Output Mode Select Circuit."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0		Selected Mode				
												SED1565***	SED1566***	SED1567***	SED1568***	SED1569***
0	1	0	1	1	0	0	0	*	*	*	Normal	COM0→COM63	COM0→COM47	COM0→COM31	COM0→COM53	COM0→COM51
							1				Reverse	COM63→COM0	COM47→COM0	COM31→COM0	COM53→COM0	COM51→COM0

* Disabled bit

Power Controller Set

This command sets the power supply circuit functions. See the function explanation in "The Power Supply Circuit," for details

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected Mode
0	1	0	0	0	1	0	1	0			Booster circuit: OFF
								1			Booster circuit: ON
									0		Voltage regulator circuit: OFF
									1		Voltage regulator circuit: ON
										0	Voltage follower circuit: OFF
										1	Voltage follower circuit: ON

[Translator's Note: the abbreviations explained within these parentheses for V and V/F have been written out in the English translation and are therefore no longer necessary.]

V_5 Voltage Regulator Internal Resistor Ratio Set

This command sets the V_5 voltage regulator internal resistor ratio. For details, see the function explanation is "The Power Supply Circuits."

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V_5 through the output from the voltage regulator circuits of the internal liquid crystal power supply. This command is a two byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

• The Electronic Volume Mode Set

When this command is input, the electronic volume register set command becomes enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal drive voltage V_5 assumes one of the 64 voltage levels.
When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	1	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

* Inactive bit

When the electronic volume function is not used, set this to (1, 0, 0, 0, 0, 0)

• The Electronic Volume Register Set Sequence

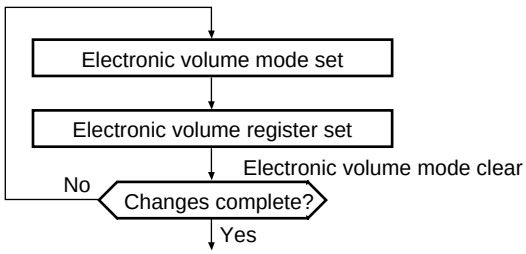


Figure 26

Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.
This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.
The static indicator ON command is a double byte command paired with the static indicator register set command, and thus one must execute one after the other. (The static indicator OFF command is a single byte command.)

• Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static Indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets two bits of data into the static indicator register, and is used to set the static indicator into a blinking mode.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately one second intervals)
									1	0	ON (blinking at approximately 0.5 second intervals)
									1	1	ON (constantly on)

* Disabled bit

• Static Indicator Register Set Sequence

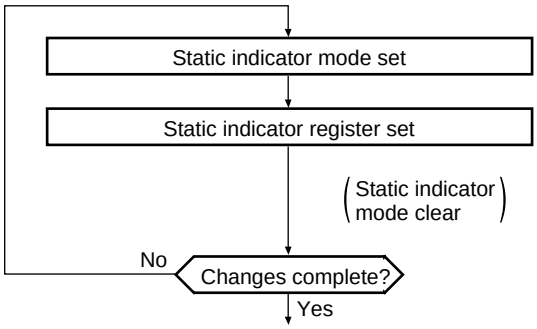


Figure 27

Power Save (Compound Command)

When the display all points ON is performed while the display is in the OFF mode, the power saver mode is entered, thus greatly reducing power consumption.
The power saver mode has two different modes: the sleep mode and the standby mode. When the static indicator is OFF, it is the sleep mode that is entered. When the static indicator is ON, it is the standby mode that is entered.
In the sleep mode and in the standby mode, the display data is saved as is the operating mode that was in effect before the power saver mode was initiated, and the MPU is still able to access the display data RAM.
Refer to figure 26 for power save off sequence.

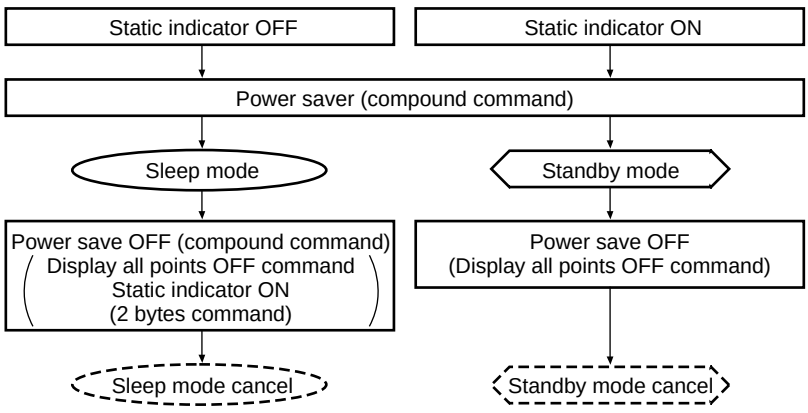


Figure 28

• Sleep Mode

This stops all operations in the LCD display system, and as long as there are no accesses from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

① The oscillator circuit and the LCD power supply circuit are halted.
② All liquid crystal drive circuits are halted, and the segment in common drive outputs output a V_{DD} level.

• Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive. The internal modes are in the following states during standby mode.

① The LCD power supply circuits are halted. The oscillator circuit continues to operate.
② The duty drive system liquid crystal drive circuits are halted and the segment and common driver outputs output a V_{DD} level. The static drive system does not operate.

When a reset command is performed while in standby mode, the system enters sleep mode.

* When an external power supply is used, it is recommended that the functions of the external power supply circuit be stopped when the power saver mode is started. For example, when the various levels of liquid crystal drive voltage are provided by external resistive voltage dividers, it is recommended that a circuit be added in order to cut the electrical current flowing through the resistive voltage divider circuit when the power saver mode is in effect. The SED1565 series chips have a liquid crystal display blanking control terminal $\overline{DOF}$. This terminal enters an "L" state when the power saver mode is launched. Using the output of $\overline{DOF}$, it is possible to stop the function of an external power supply circuit.
* When the master is turned on, the oscillator circuit is operable immediately after the powering on.

NOP

Non-OPeration Command

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Test

This is a command for IC chip testing. Please do not use it. If the test command is used by accident, it can be cleared by applying a "L" signal to the $\overline{RES}$ input by the reset command or by using an NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

* Inactive bit

Note: The SED1565 Series chips maintain their operating modes until something happens to change them. Consequently, excessive external noise, etc., can change the internal modes of the SED1565 Series chip. Thus in the packaging and system design it is necessary to suppress the noise or take measure to prevent the noise from influencing the chip. Moreover, it is recommended that the operating modes be refreshed periodically to prevent the effects of unanticipated noise.

Table 16 Table of SED1565 Series Commands

	Command	Command Code A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4)	Column address set upper bit	0	1	0	0	0	0	1	Most significant column address				Sets the most significant 4 bits of the display RAM column address.
	Column address set lower bit	0	1	0	0	0	0	0	Least significant column address				Sets the least significant 4 bits of the display RAM column address.
(5)	Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6)	Display data write	1	1	0	Write data								Writes to the display RAM
(7)	Display data read	1	0	1	Read data								Reads from the display RAM
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9)	Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10)	Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio SED1565*** ..... 0: 1/9, 1: 1/7 SED1566*** ..... 0: 1/8, 1: 1/6 SED1567*** 0: 1/6, 1: 1/5
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15)	Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction, 1: reverse direction
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17)	V_5 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb/Ra) mode
(18)	Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	
	Electronic volume register set	0	1	0	*	*	Electronic volume value						Set the V_5 output voltage electronic volume register
(19)	Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	0: OFF, 1: ON
	Static indicator register set	0	1	0	*	*	*	*	*	*	Mode		Set the flashing mode
(20)	Power saver												Display OFF and display all points ON compound command
(21)	NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22)	Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command
(23)	Test mode reset	0	1	0	1	1	1	1	0	0	0	0	Enter during the refresh sequence.

(Note) *: disabled data

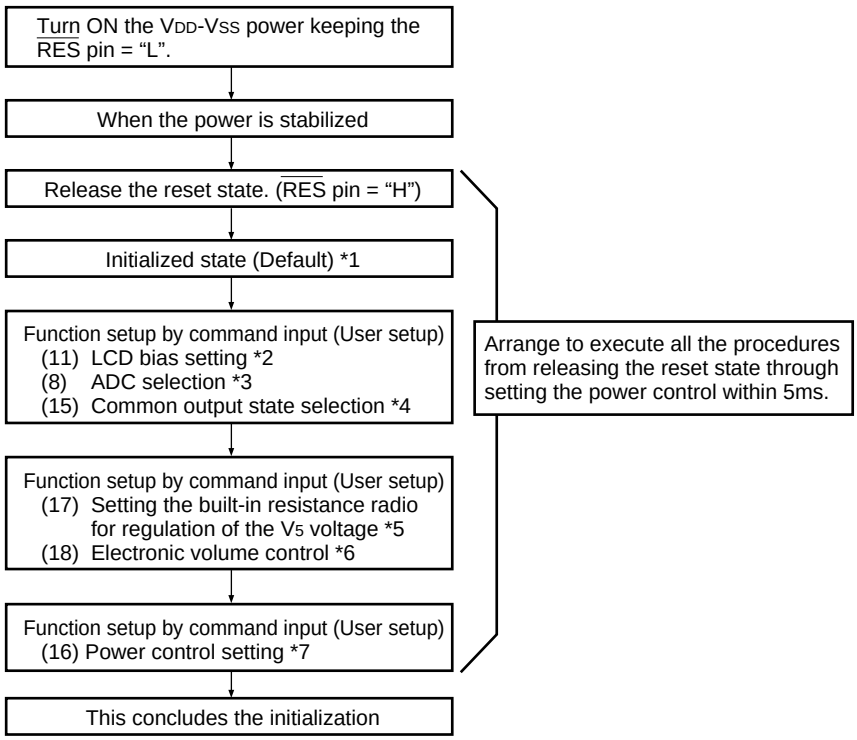
COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

(1) Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V_2 and V_3 (SEG pin) and V_1 and V_4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins ($V_1 \sim V_5$) and the V_{DD} pin, the picture on the display may become totally dark instantaneously when the power is turned on. To avoid occurrence of such a failure, we recommend the following flow when turning on the power.

① When the built-in power is being used immediately after turning on the power:



* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

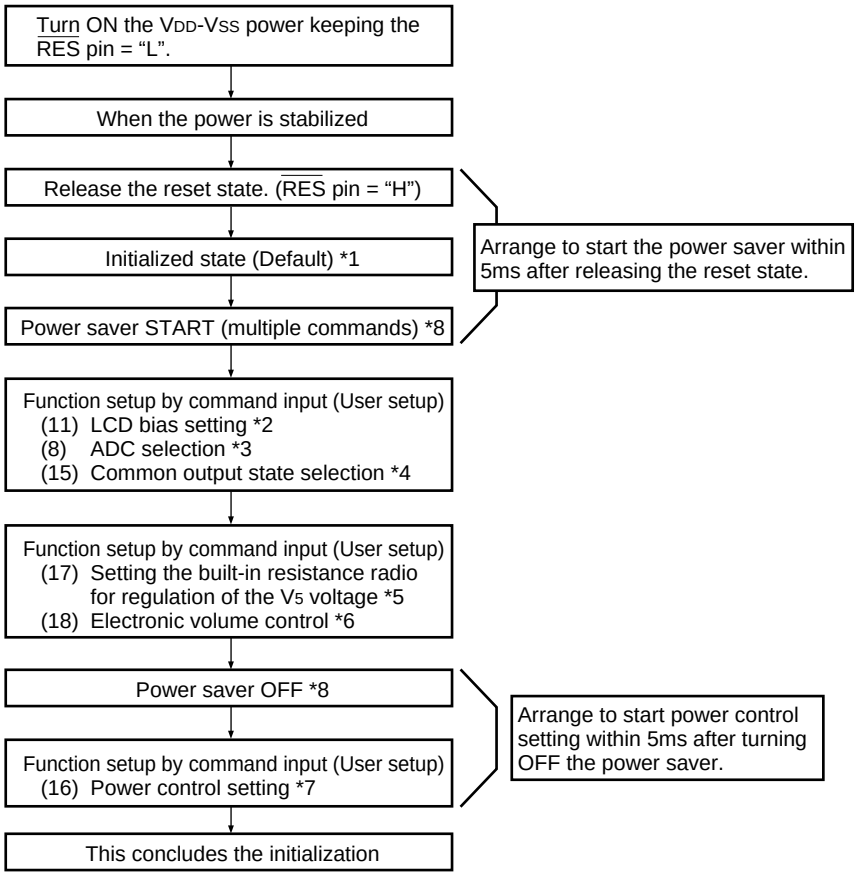
Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V_5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting

COMMAND DESCRIPTION

Instruction Setup: Reference (reference)

② When the built-in power is not being used immediately after turning on the power:

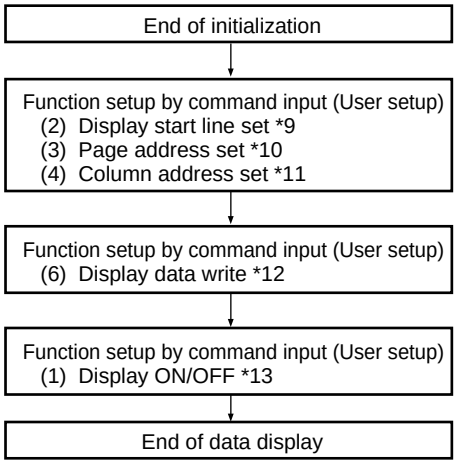


* The target time of 5ms will result to vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

Notes: Refer to respective sections or paragraphs listed below.

*1: Description of functions; Resetting circuit
*2: Command description; LCD bias setting
*3: Command description; ADC selection
*4: Command description; Common output state selection
*5: Description of functions; Power circuit & Command description; Setting the built-in resistance radio for regulation of the V5 voltage
*6: Description of functions; Power circuit & Command description; Electronic volume control
*7: Description of functions; Power circuit & Command description; Power control setting
*8: The power saver ON state can either be in sleep state or stand-by state.
Command description; Power saver START (multiple commands)

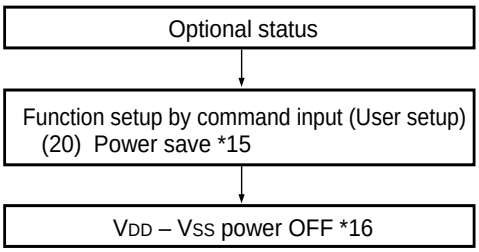
(2) Data Display



Notes: Reference items

*9: Command Description; Display start line set
*10: Command Description; Page address set
*11: Command Description; Column address set
*12: Command Description; Display data write
*13: Command Description; Display ON/OFF

(3) Power OFF *14

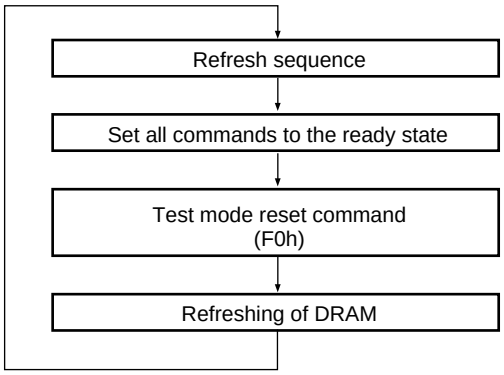


Notes: Reference items

*14: After turning OFF the internal power supply, turn OFF the power supply of this IC. (Function Description — Power Supply Circuit)
When the power of this IC is turned OFF with the internal power supply is held in the ON status, since the status where the voltage is supplied, even though an only little, to the internal LCD drive circuit is still continued, it is feared to ill affect the display quality of the LCD panel. To avoid this, be sure to observe the power OFF sequence strictly.
*15: Command Description; Power save
*16: Do not hold RESET in the ON status when power supply is off.

Refresh

It is recommended to turn on the refresh sequence regularly at a specified interval.



ABSOLUTE MAXIMUM RATINGS

Unless otherwise noted, V_{SS} = 0 V

Table 17

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		V_{DD}	–0.3 to +7.0	V
Power supply voltage (2) (V_{DD} standard)	With Triple step-up With Quad step-up	V_{SS2}	–7.0 to +0.3 –6.0 to +0.3 –4.5 to +0.3	V
Power supply voltage (3) (V_{DD} standard)		V_5, V_{OUT}	–18.0 to +0.3	V
Power supply voltage (4) (V_{DD} standard)		V_1, V_2, V_3, V_4	V_5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V_O	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP Bare chip	T_{STR}	–55 to +100 –55 to +125	°C

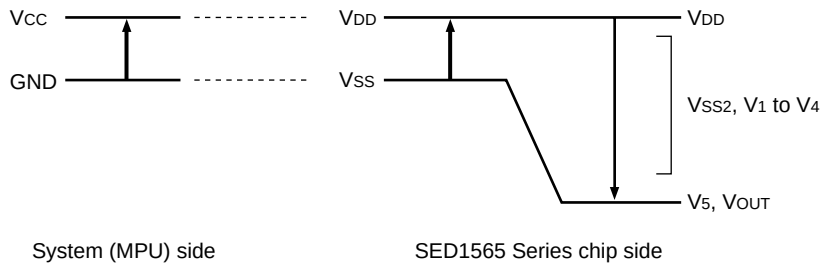


Figure 29

Notes and Cautions
1. The V_{SS2}, V_1 to V_5 and V_{OUT} are relative to the V_{DD} = 0V reference.
2. Insure that the voltage levels of V_1, V_2, V_3, and V_4 are always such that $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. Permanent damage to the LSI may result if the LSI is used outside of the absolute maximum ratings. Moreover, it is recommended that in normal operation the chip be used at the electrical characteristic conditions, and use of the LSI outside of these conditions may not only result in malfunctions of the LSI, but may have a negative impact on the LSI reliability as well.

DC CHARACTERISTICS

Unless otherwise specified, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%, Ta = –40 to 85°C

Table 18

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Operating Voltage (1)	Recommended Voltage	V_{DD}		2.7	—	3.3	V	V_{DD}*1
	Possible Operating Voltage			1.8	—	5.5	V	V_{DD}*1
Operating Voltage (2)	Recommended Voltage	V_{SS2}	(Relative to V_{DD})	–3.3	—	–2.7	V	V_{SS2}
	Possible Operating Voltage	V_{SS2}	(Relative to V_{DD})	–6.0	—	–1.8	V	V_{SS2}
Operating Voltage (3)	Possible Operating Voltage	V_5	(Relative to V_{DD})	–16.0	—	–4.5	V	V_5 *2
	Possible Operating Voltage	V_1, V_2	(Relative to V_{DD})	0.4 × V_5	—	V_{DD}	V	V_1, V_2
	Possible Operating Voltage	V_3, V_4	(Relative to V_{DD})	V_5	—	0.6 × V_5	V	V_3, V_4
High-level Input Voltage		V_{IHC}		0.8 × V_{DD}	—	V_{DD}	V	*3
Low-level Input Voltage		V_{ILC}		V_{SS}	—	0.2 × V_{DD}	V	*3
High-level Output Voltage		V_{OHC}	I_{OH} = –0.5 mA	0.8 × V_{DD}	—	V_{DD}	V	*4
Low-level Output Voltage		V_{OLC}	I_{OL} = 0.5 mA	V_{SS}	—	0.2 × V_{DD}	V	*4
Input leakage current		I_{LI}	V_{IN} = V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leakage current		I_{LO}		–3.0	—	3.0	µA	*6
Liquid Crystal Driver ON Resistance		R_{ON}	Ta = 25°C (Relative To V_{DD}) V_5 = –14.0 V	—	2.0	3.5	KΩ	SEGn
			Ta = 25°C (Relative To V_{DD}) V_5 = –8.0 V	—	3.2	5.4	KΩ	COMn *7
Static Consumption Current		I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output Leakage Current		I_{5Q}	V_5 = –18.0 V (Relative To V_{DD})	—	0.01	15	µA	V_5
Input Terminal Capacitance		C_{IN}	Ta = 25°C f = 1 MHz	—	5.0	8.0	pF	
Oscillator Frequency	Internal Oscillator	f_{OSC}	Ta = 25°C	18	22	26	kHz	*8
	External Input	f_{CL}	SED1565★★★/1567★★★	18	22	26	kHz	CL
	Internal Oscillator	f_{OSC}	Ta = 25°C	27	33	39	kHz	*8
	External Input	f_{CL}	SED1566★★★/1568★★★/1569★★★	14	17	20	kHz	CL

Table 19

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Internal Power	Input voltage	V_{SS2}	With Triple (Relative To V_{DD})		–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	With Quad (Relative To V_{DD})		–4.5	—	–1.8	V	V_{SS2}
	Supply Step-up output voltage Circuit	V_{OUT}	(Relative to V_{DD})		–18.0	—	—	V	V_{OUT}
	Voltage regulator Circuit Operating Voltage	V_{OUT}	(Relative to V_{DD})		–18.0	—	–6.0	V	V_{OUT}
	Voltage Follower Circuit Operating Voltage	V_5	(Relative to V_{DD})		–16.0	—	–4.5	V	V_5 *9
	Base Voltage	V_{REG0}	Ta = 25°C	–0.05%/°C	–2.04	–2.10	–2.16	V	*10
		V_{REG1}	(Relative to V_{DD})	–0.2%/°C	–4.65	–4.9	–5.15	V	*10

• Dynamic Consumption Current (1), During Display, with the Internal Power Supply OFF
Current consumed by total ICs when an external power supply is used.

Table 20 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★★★	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	18	30	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	16	27		
SED1566★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	13	22		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	19		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	9	15		
SED1567★★★		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	8	13		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	7	12		
SED1568★★★/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
SED1569★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		

Table 21 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
SED1565★★★	I_{DD} (1)	V_{DD} = 5.0 V, V_5 – V_{DD} = –11.0 V	—	23	38	µA	*11
		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	21	35		
SED1566★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –11.0 V	—	17	29		
		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	14	24		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	12	20		
SED1567★★★		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	11	18		
		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	10	17		
SED1568★★★/		V_{DD} = 5.0 V, V_5 – V_{DD} = –8.0 V	—	15	25		
SED1569★★★		V_{DD} = 3.0 V, V_5 – V_{DD} = –8.0 V	—	13	22		

• Dynamic Consumption Current (2), During Display, with the Internal Power Supply ON

Table 22 Display Pattern OFF

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SED1565★★★	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	67	112	µA	*12
			High-Power Mode	—	114	190		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	81	135		
			High-Power Mode	—	138	230		
SED1566★★★		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	35	59		
			High-Power Mode	—	64	107		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	43	72		
			High-Power Mode	—	84	140		
		V_{DD} = 3.0 V, Quad step-up voltage. V_5 – V_{DD} = –11.0 V	Normal Mode	—	72	121		
			High-Power Mode	—	128	214		
SED1567★★★		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	26	44		
			High-Power Mode	—	60	100		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	29	49		
			High-Power Mode	—	73	122		
SED1568★★★/		V_{DD} = 5.0 V, Double step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	37	62		
SED1569★★★			High-Power Mode	—	67	112		
		V_{DD} = 3.0 V, Triple step-up voltage. V_5 – V_{DD} = –8.0 V	Normal Mode	—	46	77		
			High-Power Mode	—	87	145		

Table 23 Display Pattern Checker

Ta = 25°C

Item	Symbol	Condition		Rating			Units	Notes
				Min.	Typ.	Max.		
SED1565★★★	I_{DD} (2)	V_{DD} = 5.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	81	135	µA	*12
			High-Power Mode	—	127	212		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	96	160		
			High-Power Mode	—	153	255		
SED1566★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	41	69		
			High-Power Mode	—	71	119		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	51	85		
			High-Power Mode	—	92	154		
		V_{DD} = 3.0 V, Quad step-up voltage. $V_5 - V_{DD}$ = –11.0 V	Normal Mode	—	85	142		
			High-Power Mode	—	142	237		
SED1567★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	32	53		
			High-Power Mode	—	62	103		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	73		
			High-Power Mode	—	89	148		
SED1568★★★/ SED1569★★★		V_{DD} = 5.0 V, Double step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	44	74		
			High-Power Mode	—	74	127		
		V_{DD} = 3.0 V, Triple step-up voltage. $V_5 - V_{DD}$ = –8.0 V	Normal Mode	—	54	90		
			High-Power Mode	—	95	159		

• Consumption Current at Time of Power Saver Mode, V_{SS} = 0 V, V_{DD} = 3.0 V ± 10%

Table 24

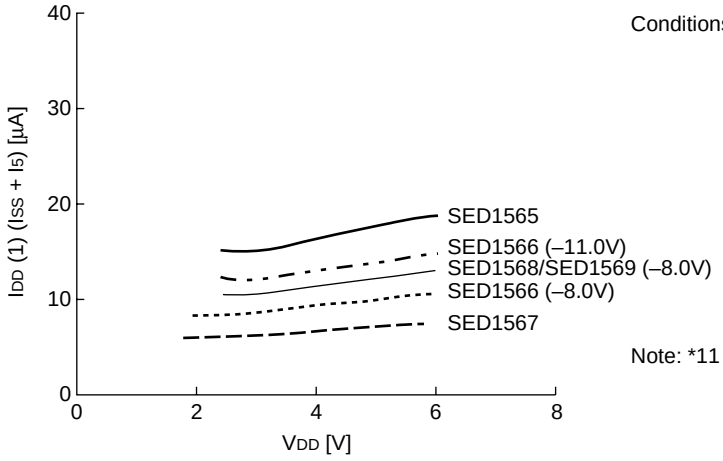
Ta = 25°C

Item		Symbol	Condition	Rating			Units	Notes
				Min.	Typ.	Max.		
Sleep mode	SED1565★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1565★★★	I_{DDS2}	—		4	8	µA	
Sleep mode	SED1566★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1566★★★	I_{DDS2}	—		4	8	µA	
Sleep mode	SED1567★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1567★★★	I_{DDS2}	—		3	6	µA	
Sleep mode	SED1568★★★/ SED1569★★★	I_{DDS1}	—		0.01	5	µA	
Standby Mode	SED1568★★★/ SED1569★★★	I_{DDS2}	—		4	8	µA	

TBD: To Be Determined

Reference Data 1

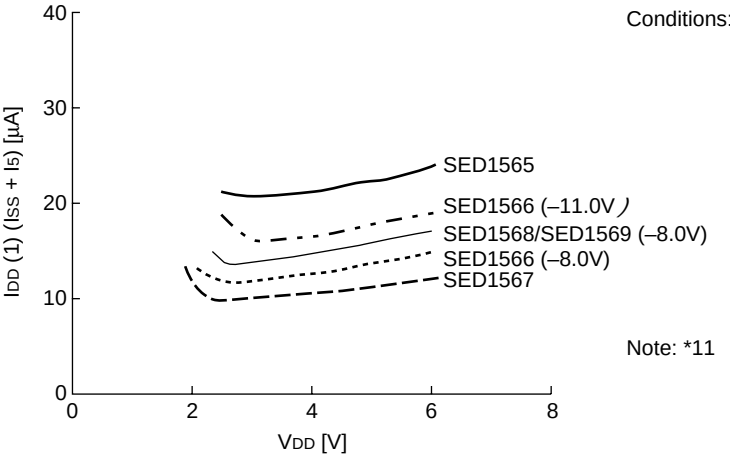
- Dynamic Consumption Current (1) During LCD Display Using an External Power Supply



Conditions: Internal power supply OFF
External power supply in use
SED1565/SED1566 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
SED1566 (–8.0V)/SED1567:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: OFF
Ta = 25°C

Note: *11

Figure 30



Conditions: Internal power supply OFF
External power supply in use
SED1565/SED1566 (–11.0V):
$V_5 – V_{DD}$ = –11.0 V
SED1566 (–8.0V)/SED1567:
$V_5 – V_{DD}$ = –8.0 V
Display pattern: Checker
Ta = 25°C

Note: *11

Figure 31

Reference Data 2

- Dynamic Consumption Current (2) During LCD display using the internal power supply

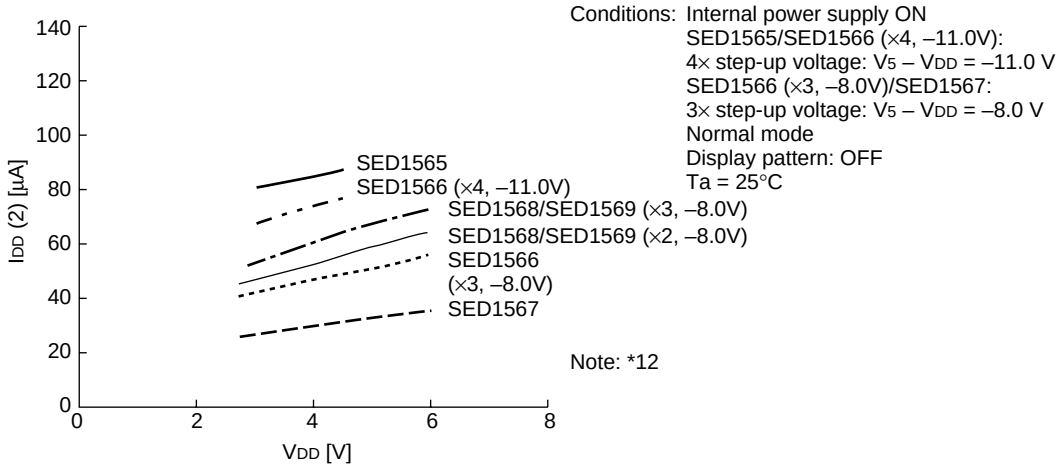


Figure 32

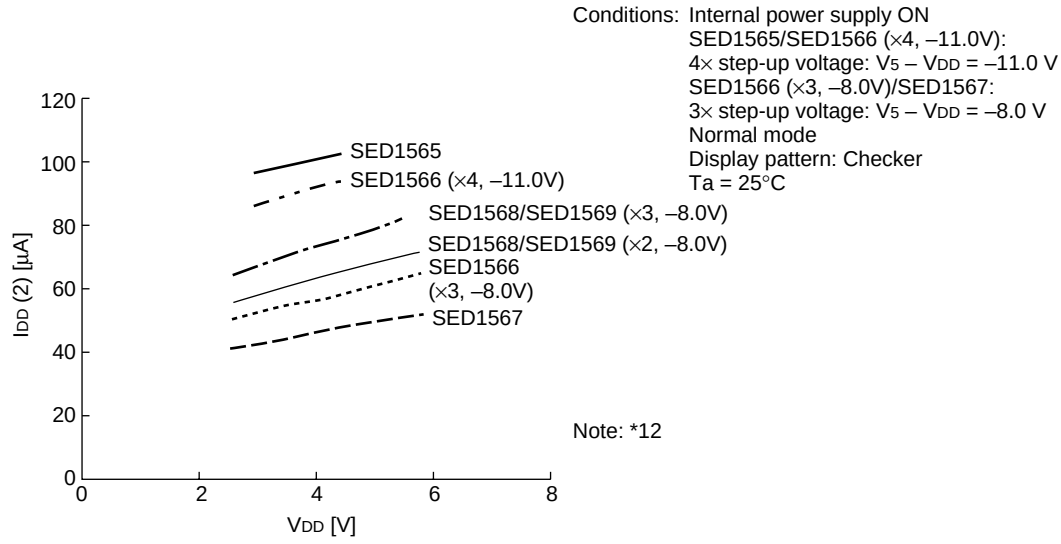
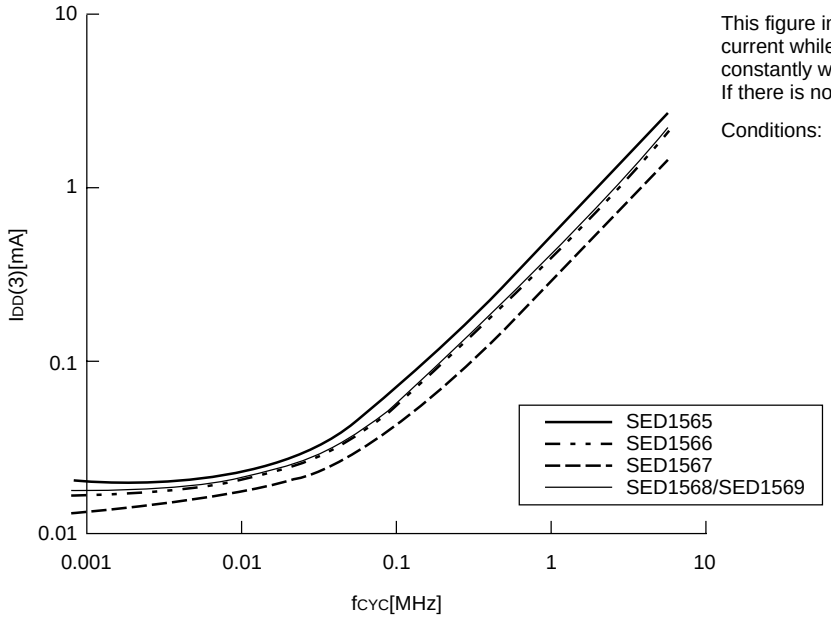


Figure 33

Reference Data 3

• Dynamic Consumption Current (3) During access



This figure indicates the consumption current while the checker pattern is constantly written through f_{CYC}.
If there is no access, then only (1) remains.

Conditions: Internal power supply OFF, external power supply used
SED1565:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–11.0 V
SED1566/SED1567:
$V_{DD} - V_{SS}$ = 3.0 V, V_5=–8.0 V
Ta = 25°C

Figure 34

Reference Data 4

• Operating voltage range of V_{SS} and V_5 systems

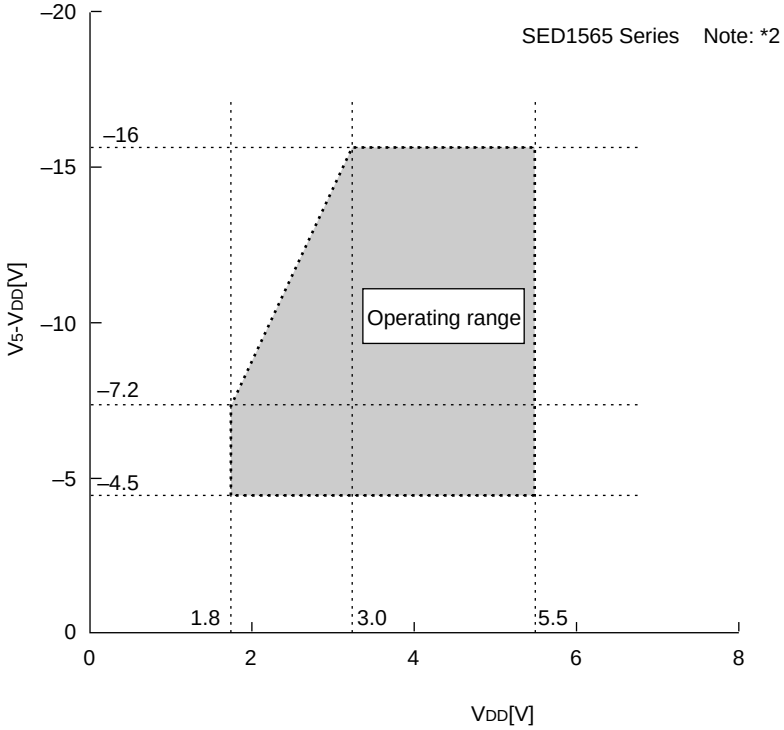


Figure 35

- The Relationship Between Oscillator Frequency f_{OSC}, Display Clock Frequency f_{CL} and the Liquid Crystal Frame Rate Frequency f_{FR}

Table 25

Item		f_{CL}	f_{FR}
SED1565***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4 \times 65}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{260}$
SED1566***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 49}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{196}$
SED1567***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 33}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{264}$
SED1568***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 55}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{220}$
SED1569***	When the internal oscillator circuit is used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8 \times 53}$
	When the internal oscillator circuit is not used	External input (f_{CL})	$\frac{f_{CL}}{212}$

(f_{FR} is the liquid crystal alternating current period, and not the FR signal period.)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The operating voltage range for the V_{DD} system and the V_5 system is as shown in Figure 33. This applies when the external power supply is being used.

*3 The A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*4 The D0 to D7, FR, FRS, $\overline{DOF}$, and CL terminals.

*5 The A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS, and $\overline{HPM}$ terminals.

*6 Applies when the D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ terminals are in a high impedance state.

*7 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V_1, V_2, V_3, and V_4). These are specified for the operating voltage (3) range.
R_{ON} = 0.1 V/Δ I (Where Δ I is the current that flows when 0.1 V is applied while the power supply is ON.)

*8 See Table 9-7 for the relationship between the oscillator frequency and the frame rate frequency.

*9 The V_5 voltage regulator circuit regulates within the operating voltage range of the voltage follower.

*10 This is the internal voltage reference supply for the V_5 voltage regulator circuit. In the SED1565 Series chips, the temperature range can come in three types as V_{REG} options: (1) approximately –0.05%/°C, (2) –0.2%/°C, and (3) external input.

*11, 12 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.
The SED1565 is 1/9 biased, SED1566 is 1/8 biased and SED1567 is 1/6 biased.
Does not include the current due to the LCD panel capacity and wiring capacity.
Applicable only when there is no access from the MPU.

*12 It is the value on a model having the V_{REG} option temperature gradient is –0.05%/°C when the V_5 voltage regulator internal resistor is used.

TIMING CHARACTERISTICS

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

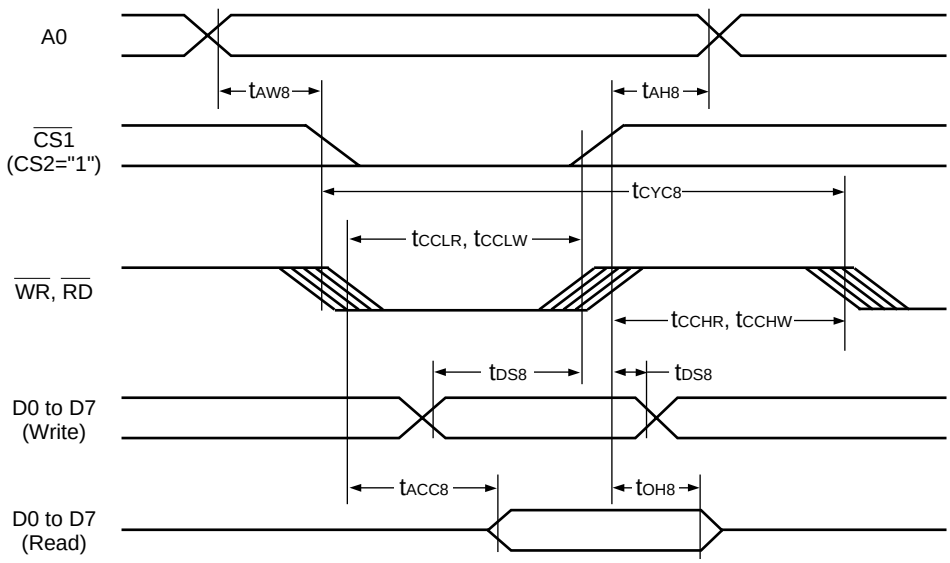


Figure 36

Table 26

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		166	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		30	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		70	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		30	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		30	—	ns
Data setup time	D0 to D7	t_{DS8}		30	—	ns
Address hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	70	ns
Output disable time		t_{OH8}		5	50	ns

Table 27

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		300	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		60	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		120	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		60	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		60	—	ns
Data setup time	D0 to D7	t_{DS8}		40	—	ns
Address hold time		t_{DH8}		15	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	140	ns
Output disable time		t_{OH8}		10	100	ns

Table 28

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	ns
System cycle time	A0	t_{CYC8}		1000	—	ns
Control L pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCLW}		120	—	ns
Control L pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCLR}		240	—	ns
Control H pulse width ($\overline{WR}$)	$\overline{WR}$	t_{CCHW}		120	—	ns
Control H pulse width ($\overline{RD}$)	$\overline{RD}$	t_{CCHR}		120	—	ns
Data setup time	D0 to D7	t_{DS8}		80	—	ns
Address hold time		t_{DH8}		30	—	ns
$\overline{RD}$ access time		t_{ACC8}	C_L = 100 pF	—	280	ns
Output disable time		t_{OH8}		10	200	ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLW} – t_{CCHW}$) for ($t_r + t_f$) ≤ ($t_{CYC8} – t_{CCLR} – t_{CCHR}$) are specified.

*2 All timing is specified using 20% and 80% of V_{DD} as the reference.

*3 t_{CCLW} and t_{CCLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and $\overline{WR}$ and $\overline{RD}$ being at the "L" level.

System Bus Read/Write Characteristics 2 (6800 Series MPU)

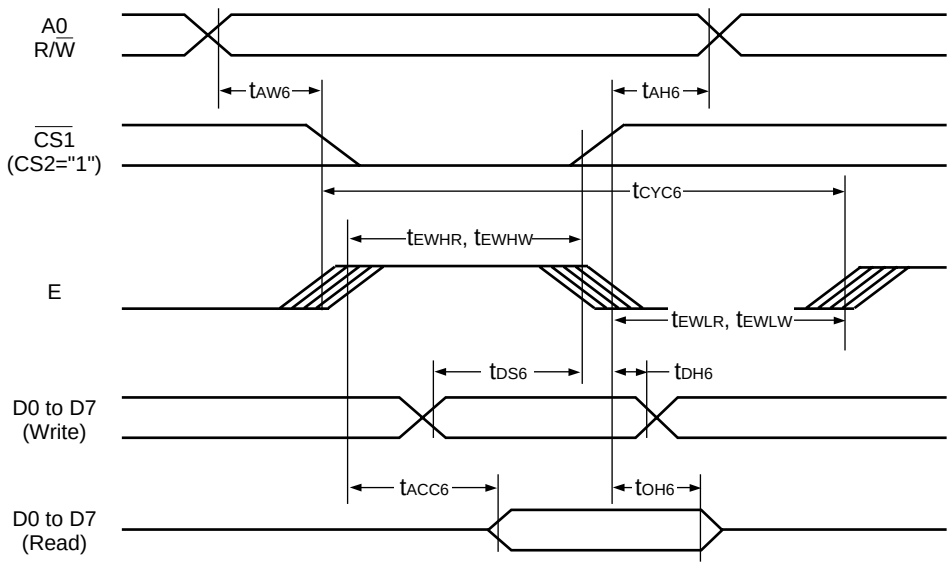


Figure 37

Table 29

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	ns
System cycle time		A0	t_{CYC6}		166	—	ns
Data setup time		D0 to D7	t_{DS6}		30	—	ns
Data hold time			t_{DH6}		10	—	ns
Access time			t_{ACC6}	C_L = 100 pF	—	70	ns
Output disable time			t_{OH6}		10	50	ns
Enable H pulse time	Read	E	t_{EWHR}		70	—	ns
	Write		t_{EWHW}		30	—	ns
Enable L pulse time	Read	E	t_{EWLR}		30	—	ns
	Write		t_{EWLW}		30	—	ns

Table 30

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		300	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 15	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	140 100	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		120 60	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		60 60	— —	ns ns

Table 31

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns ns
System cycle time		A0	t_{CYC6}		1000	—	ns
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		80 30	— —	ns ns
Access time Output disable time			t_{ACC6} t_{OH6}	C_L = 100 pF	— 10	280 200	ns ns
Enable H pulse time	Read Write	E	t_{EWHR} t_{EWHW}		240 120	— —	ns ns
Enable L pulse time	Read Write	E	t_{EWLR} t_{EWLW}		120 120	— —	ns ns

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLW} – t_{EWHW}$) for ($t_r + t_f$) ≤ ($t_{CYC6} – t_{EWLR} – t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being “L” (CS2 = “H”) and E.

The Serial Interface

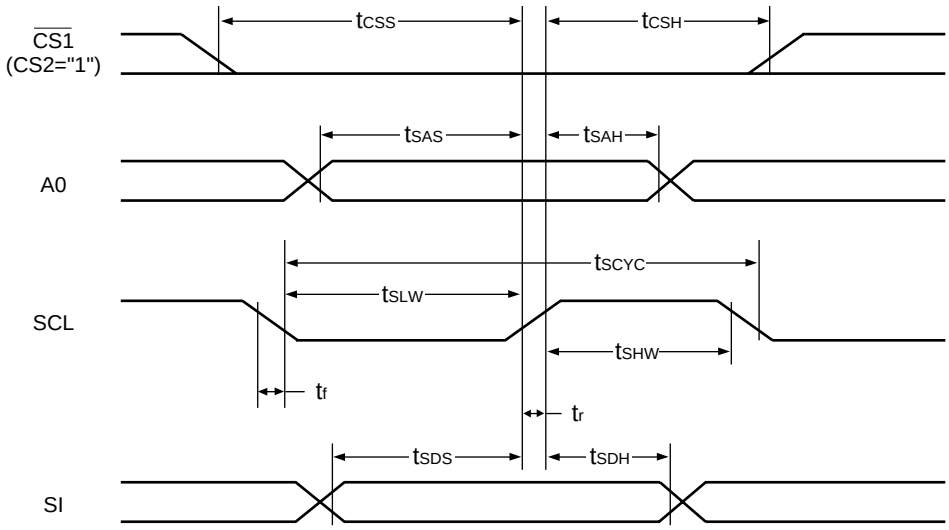


Figure 38

Table 32

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		200	—	ns
SCL “H” pulse width		t_{SHW}		75	—	ns
SCL “L” pulse width		t_{SLW}		75	—	ns
Address setup time	A0	t_{SAS}		50	—	ns
Address hold time		t_{SAH}		100	—	ns
Data setup time	SI	t_{SDS}		50	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}		100	—	ns
		t_{CSH}		100	—	ns

Table 33

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		250	—	ns
SCL “H” pulse width		t_{SHW}		100	—	ns
SCL “L” pulse width		t_{SLW}		100	—	ns
Address setup time	A0	t_{SAS}		150	—	ns
Address hold time		t_{SAH}		150	—	ns
Data setup time	SI	t_{SDS}		100	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		150	—	ns
		t_{CSH}		150	—	ns

Table 34

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min	Max	
Serial Clock Period	SCL	t_{SCYC}		400	—	ns
SCL “H” pulse width		t_{SHW}		150	—	ns
SCL “L” pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		250	—	ns
Data setup time	SI	t_{SDS}		150	—	ns
Data hold time		t_{SDH}		150	—	ns
CS-SCL time	CS	t_{CSS}		250	—	ns
		t_{CSH}		250	—	ns

*1 The input signal rise and fall time (t_r, t_f) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of V_{DD} as the standard.

Display Control Output Timing

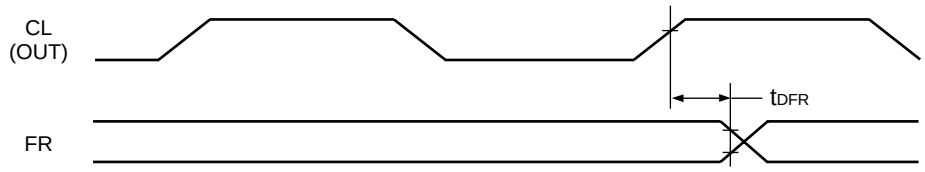


Figure 39

Table 35

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	10	40	ns

Table 36

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	20	80	ns

Table 37

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
FR delay time	FR	t_{DFR}	C_L = 50 pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timing is based on 20% and 80% of V_{DD}.

Reset Timing

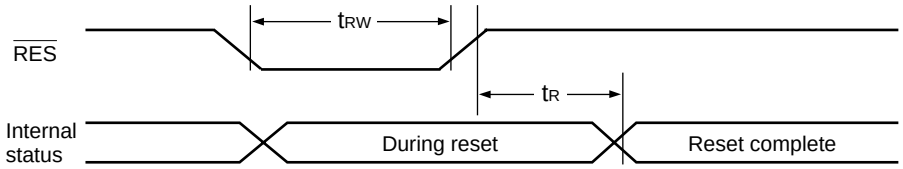


Figure 40

Table 38

(V_{DD} = 4.5 V to 5.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	0.5	µs
Reset “L” pulse width	RES	t_{RW}		0.5	—	—	µs

Table 39

(V_{DD} = 2.7 V to 4.5 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	1	µs
Reset “L” pulse width	RES	t_{RW}		1	—	—	µs

Table 40

(V_{DD} = 1.8 V to 2.7 V, Ta = –40 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min	Typ	Max	
Reset time		t_R		—	—	1.5	µs
Reset “L” pulse width	RES	t_{RW}		1.5	—	—	µs

*1 All timing is specified with 20% and 80% of V_{DD} as the standard.

THE MPU INTERFACE (REFERENCE EXAMPLES)

The SED1565 Series can be connected to either 80 × 86 Series MPUs or to 68000 Series MPUs. Moreover, using the serial interface it is possible to operate the SED1565 series chips with fewer signal lines.
The display area can be enlarged by using multiple SED1565 Series chips. When this is done, the chip select signal can be used to select the individual ICs to access.

(1) 8080 Series MPUs

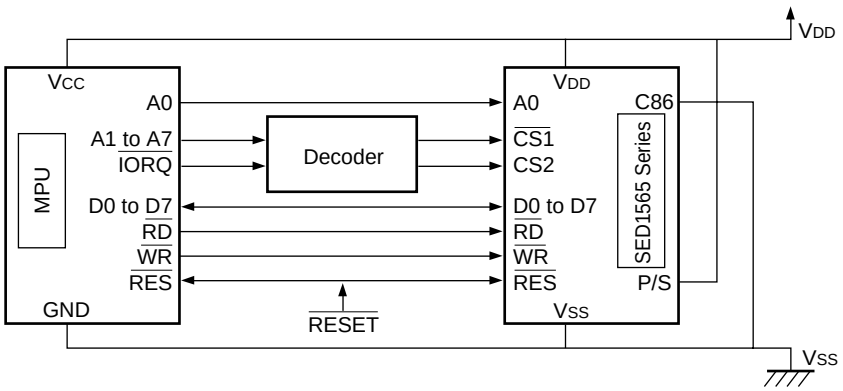


Figure 41-1

(2) 6800 Series MPUs

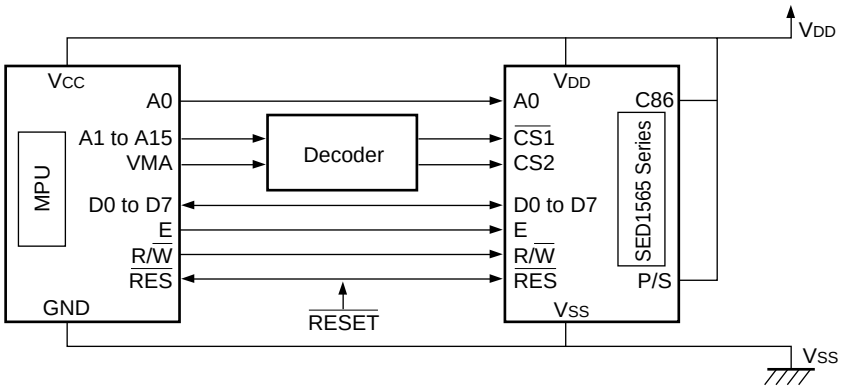


Figure 41-2

(3) Using the Serial Interface

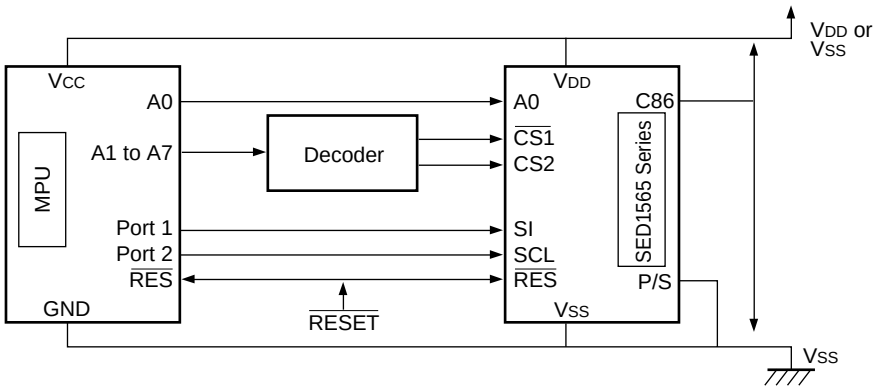


Figure 41-3

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLE)

The liquid crystal display area can be enlarged with ease through the use of multiple SED1565 Series chips. Use a same equipment type.

(1) SED1565 (master) ↔ SED1565 (slave)

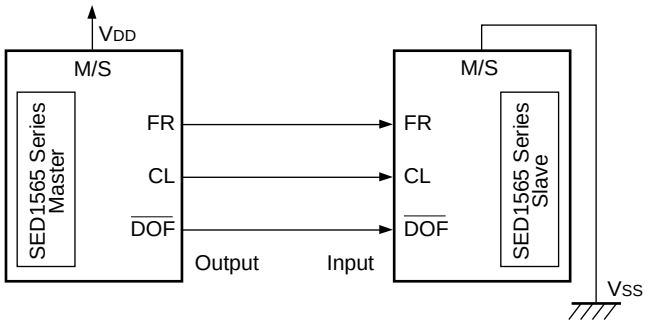


Figure 42

CONNECTIONS BETWEEN LCD DRIVERS (REFERENCE EXAMPLES)

The liquid crystal display area can be enlarged with ease through the use of multiple SED1565 Series chips. Use a same equipment type, in the composition of these chips.

(1) Single-chip Structure

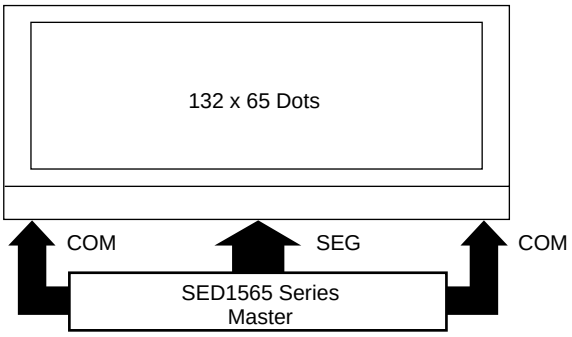


Figure 43-1

(2) Double-chip Structure, #1

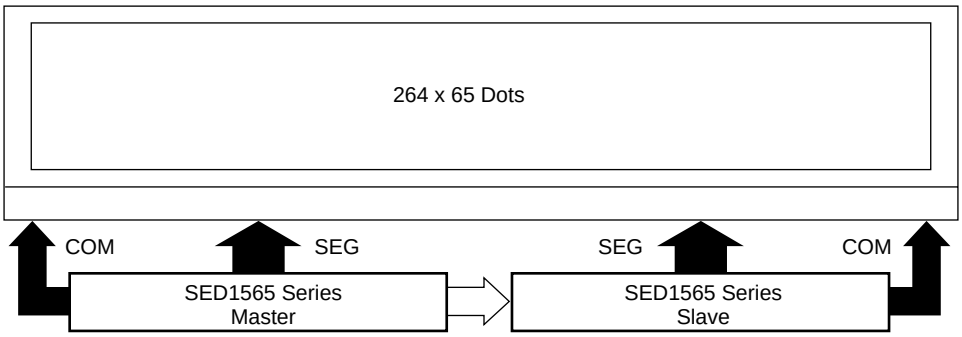
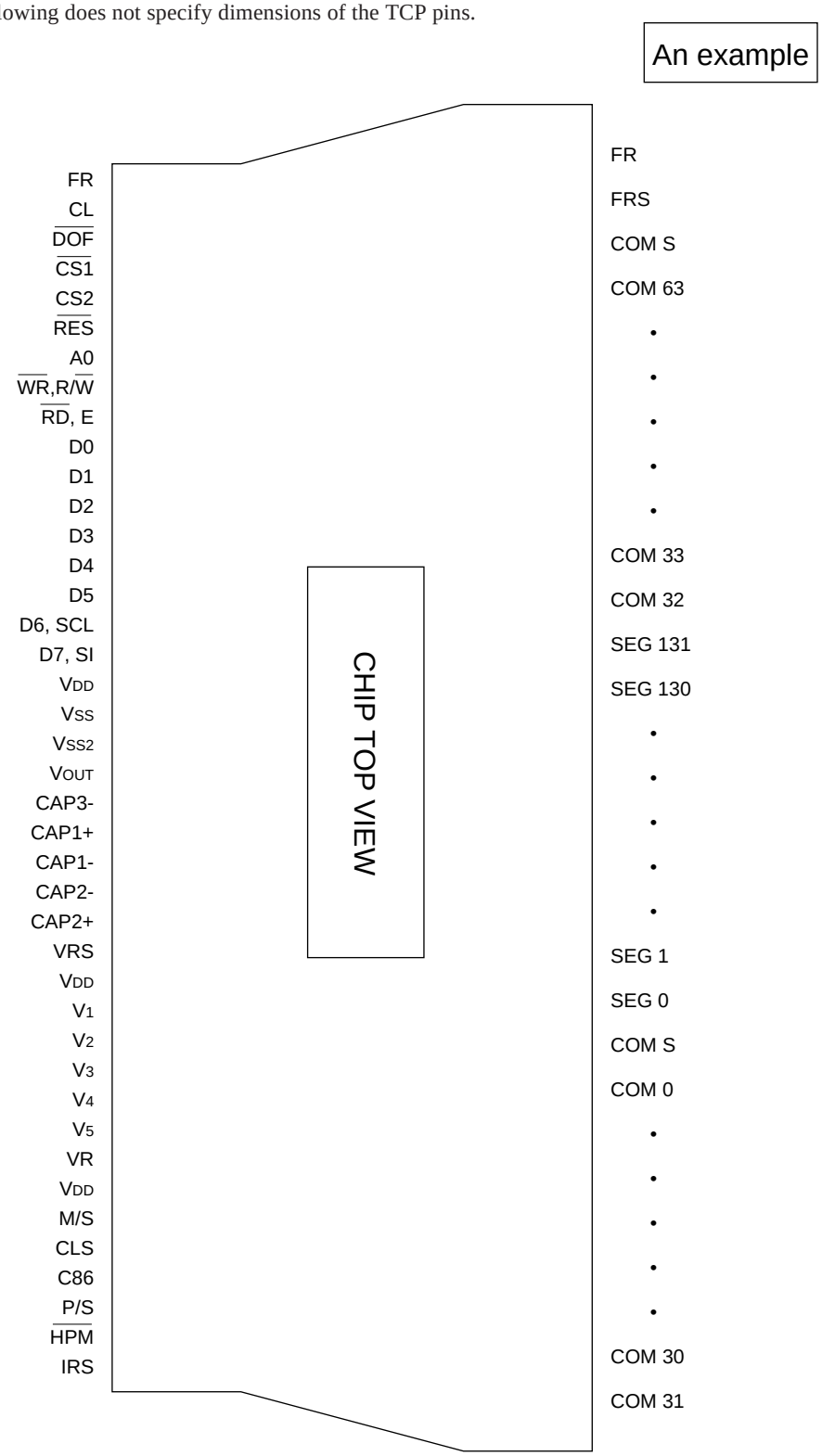


Figure 43-2

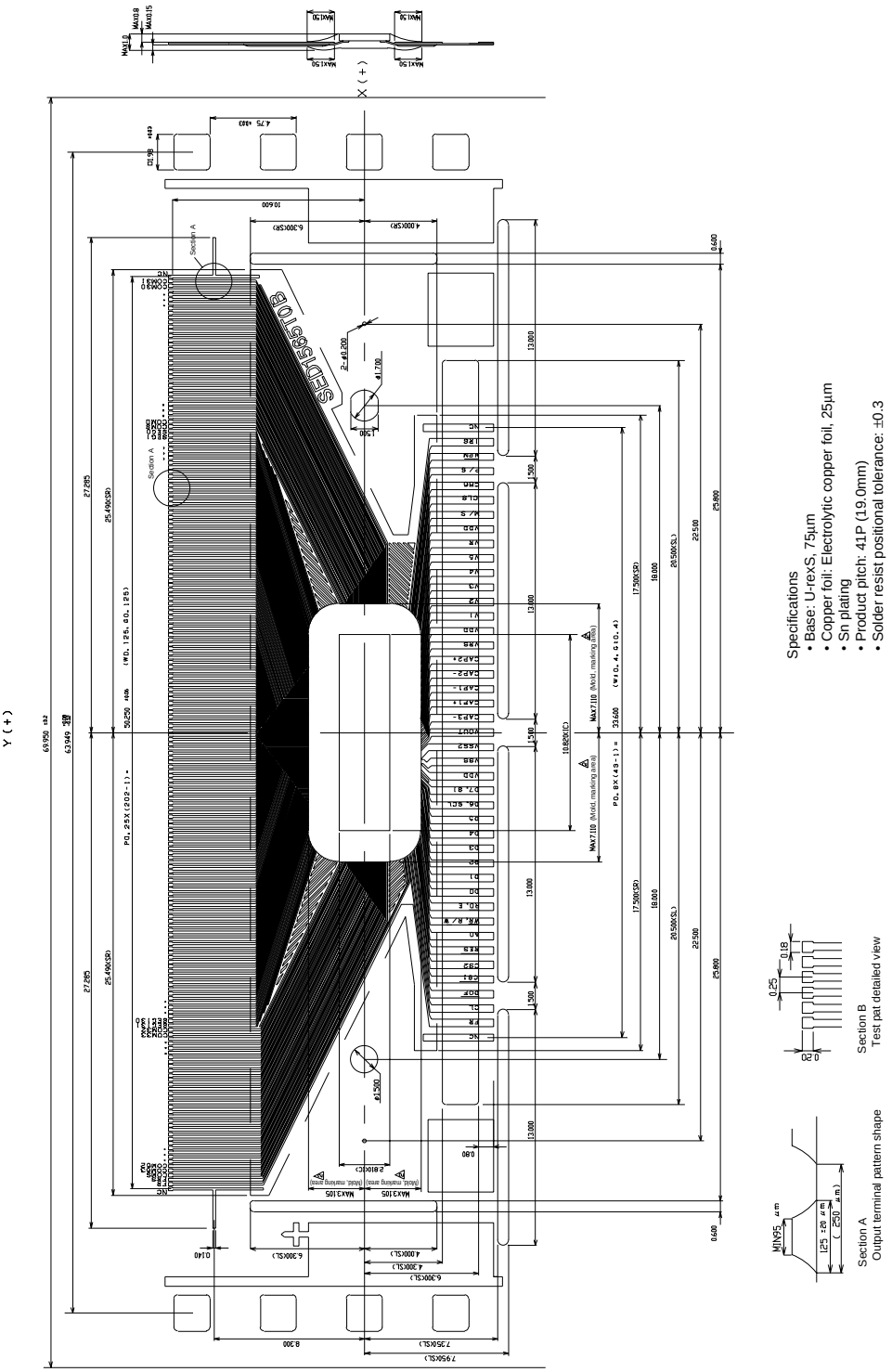
A SAMPLE TCP PIN ASSIGNMENT

SED1565T0B TCP Pin Layout

Note: The following does not specify dimensions of the TCP pins.



EXTERNAL VIEW OF TCP PINS



NOTICE

Please be advised on the following points in the use of this development manual.

1. This manual is subject to change without previous notice.
2. This manual does not guarantee or furnish the industrial property right nor its execution.
   Application examples in the manual are intended to ensure your better understanding of the product. Thus, the manufacturer shall not be liable for any trouble arising in your circuits from using such application example.
   Numerical values provided in the property table of this manual are represented with their magnitude on the numerical line.
3. No part of this manual may not be reproduced, copied or used for commercial purposes without a written permission from the manufacturer.

In handling of semiconductor devices, your attention is required to the following points.

[Precautions on Light]

Property of semiconductor devices may be affected when they are exposed to light, possibly resulting in malfunctioning of the ICs. To prevent such malfunctioning of the ICs mounted on the boards or products, make sure that:

(1) Your design and mounting layout done are so that the IC is not exposed to light in actual use.
(2) The IC is protected from light in the inspection process.
(3) The IC is protected from light in its front, rear and side faces.