LMG638X FAMILY

- 256 dot (W) x 64 dot (H) graphic and alphanumeric display
- Controller HD61830 built-in
- Colour Tone :
  LMG6380QHGR - blue on grey
  LMG6381QHGE - blue on grey with EL Backlight
  LMG6382QHFR - reflective film B/W type

MECHANICAL DATA (Nominal Dimensions)

Module size	160W x 68H x 9.5D (max) mm
Effective display area	126.3W x 37H mm
Dot size	0.44W x 0.44H mm
Dot pitch	0.47W x 0.47H mm
Viewing direction	6 o'clock
Weight	about 115g
Duty	1 / 64

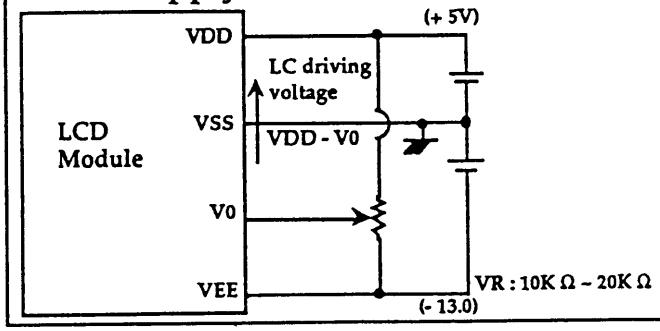
ABSOLUTE MAXIMUM RATINGS

	min	max
Power supply for logic (VDD - VSS)	0	7.0 V
Power supply for LCD drive (VDD - VSS)	0	22.0 V
Input Voltage (Vi)	VSS	VDD V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	-20	60°C

Pin Assignment

PIN NO.	SYMBOL	FUNCTION
A1	VSS	Ground
A2	VDD	Power supply for logic
A3	V0	Power supply for LCD drive
A4	RS	Register select
A5	R / W	Read / write
A6	E	Enable
A7 - 14	DB0 - DB7	Data bus
A15	CS	Chip select
A16	RES	Reset
A17	VEE	Power supply for LCD
A18 - 20	N.C	No connection
E1	VEL	EL driving voltage
E2	VEL	EL driving voltage

Power Supply

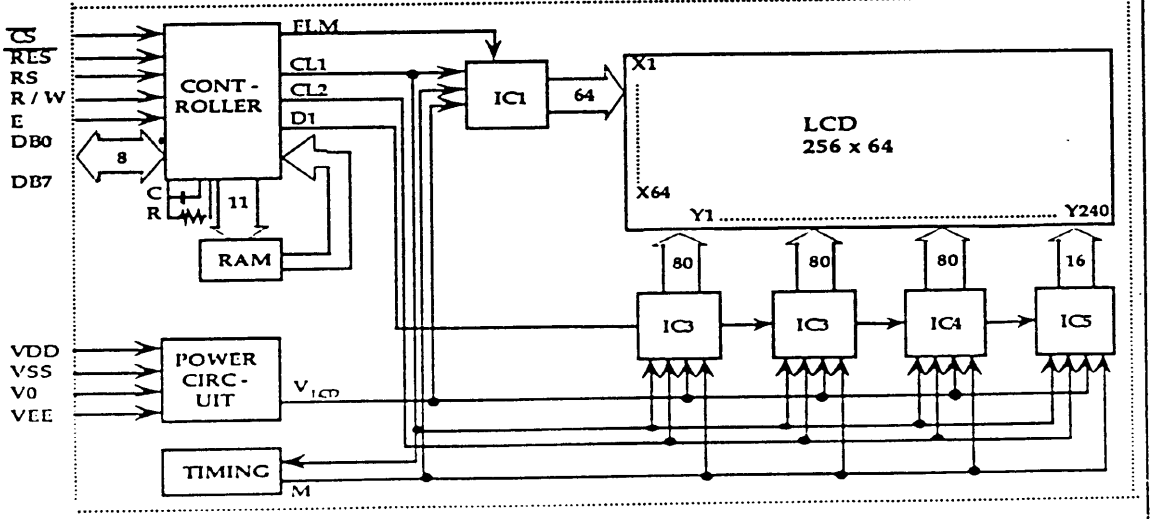


Electrical Characteristics

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Logic circuit power supply voltage		VDD - VSS		4.75	5	5.25	V
LC driver circuit power supply voltage		VEE - VSS		-12.5	-13	-13.5	V
Input voltage Note 1	H	ViH		0.8XUDD	-	VDD	V
	L	ViL		0	-	0.2XUDD	V
Input leak current		Iin		-5	-	5	μA
Output leak current		Iout		-10	-	10	
Clock frequency Note 2		fCL2		-	-	1.2	MHz
Power consumption		PW	VDD = 5.0V Ta = 25°C	-	-	250	mW
Recommended LC driving voltage Note 3		VDD - V0	Ta = 0°C	-	16.2	-	V
		ø = 0°	Ta = 25°C	-	15.3	-	
		Ø = 10°C	Ta = 40°C	-	14.7	-	
EL power supply Note 4		VEL	fEL = 400Hz	-	100	-	Vrms
		IEL	VEL = 100Vrms fEL = 400Hz	-	6	-	mArms

Note 1 : Applied to DB0 ~ DB7, CS, E, R / W, RS
Note 2 : Internal clock
Note 3 : Recommended LC driving voltage may fluctuate about ± 0.5V by each module
Note 4 : Recommended EL inverter : Pacel type - P4

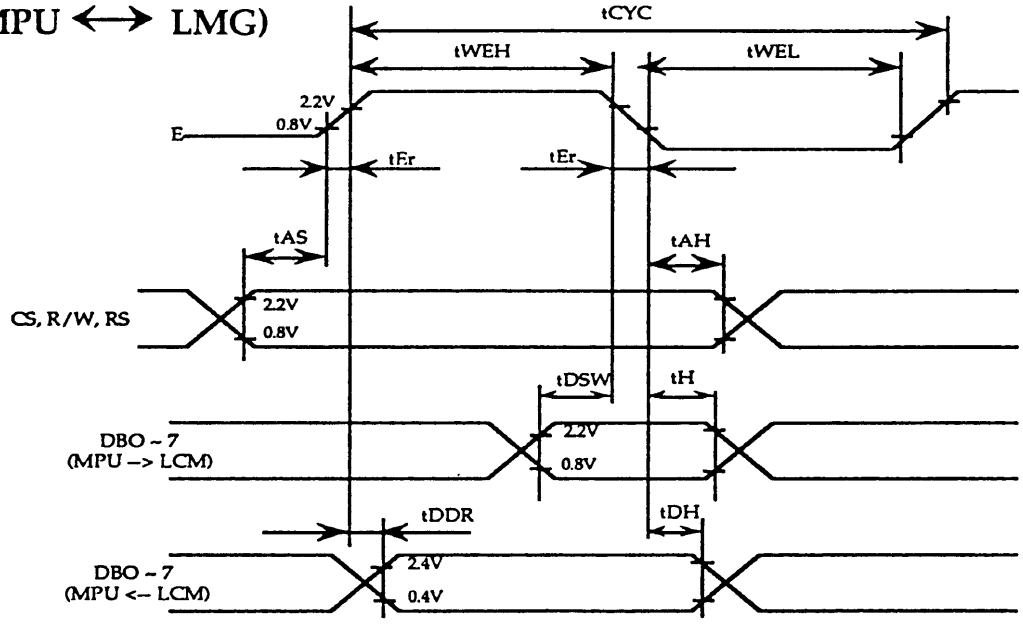
Block Diagram



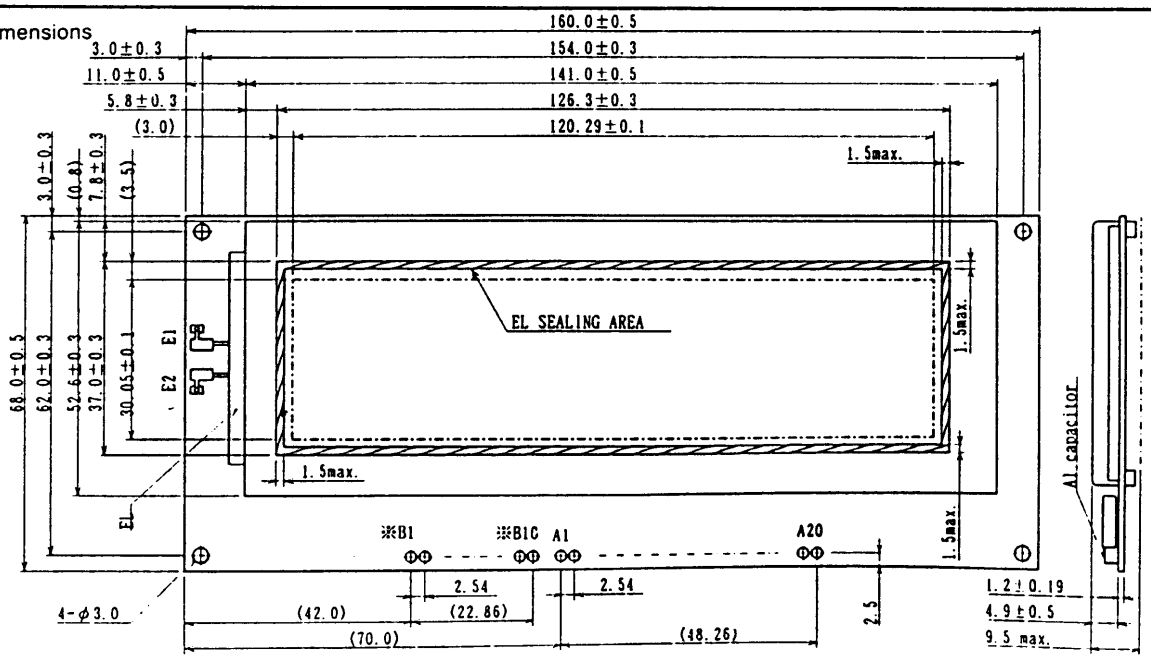
Interface Timing

ITEM		SYMBOL	MIN.	TYP.	MAX.	UNIT
Enable cycle time		tCYC	1	-	-	us
Enable pulse width	"High" level	tWEH	0.45	-	-	us
	"Low" level	tWEL	0.45	-	-	us
Enable rise time		tEr	-	-	25	ns
Enable fall time		tEf	-	-	25	ns
Setup time		tAS	140	-	-	ns
Data setup time		tDSW	225	-	-	ns
Data delay time		tDDR	-	-	225	ns
Data hold time		tH	10	-	-	ns
Address hold time		tAH	10	-	-	ns
Data hold time		tDH	20	-	-	ns

Interface Timing (MPU ⟷ LMG)



External Dimensions



Unit : mm
Scale : NTS

VIEWING DIRECTION

※B1~B10 pads should not be used.
Do not connect any signals to these pads.
Use A1~A20 for interface.