riscv-dbg

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b118d75 · 2 weeks ago

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src	dm_csrs: Replace fifo_…	2 months ago
sva	Fixed enumeration name	6 years ago
tb	dm_csrs: Replace fifo_…	2 months ago
.gitignore	Address code review nits	4 years ago
.travis.yml	Add tb running dm+ri5c…	6 years ago
Bender.yml	Bump to latest commo…	4 years ago
CHANGELOG.md	Update CHANGELOG.…	3 months ago
LICENSE	Fork from Ariane	8 years ago
LICENSE.SiFive	Add SiFive license for …	7 years ago
README.md	README.md: Add jtag …	2 years ago
src_files.yml	Merge pull request #66…	6 years ago

About

RISC-V Debug Support for our PULP RISC-V Cores

#riscv #debug

Readme

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No packages published

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RISC-V Debug Support for various Cores

This module is an implementation of a debug unit compliant with the RISC-V debug specification v0.13.1. It is used in the cva6, cv32e40p and ibex cores.

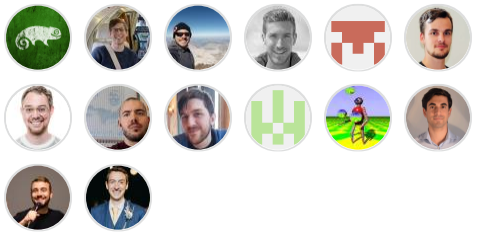
Implementation

We use an execution-based technique, also described in the specification, where the core is running in a "park loop". Depending on the request made to the debug unit via JTAG over the Debug Transport Module (DTM), the code that is being executed is changed dynamically. This approach simplifies the implementation side of the core, but means that the core is in fact always busy looping while debugging.

Features

The following features are currently supported

- Parametrizable buswidth for `XLEN=32` `XLEN=64` cores
- Accessing registers over abstract command
- Program buffer
- System bus access (only `XLEN`)



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Languages

- **SystemVerilog** 64.2%
- **C** 19.5%
- **Makefile** 4.3%
- **Linker Script** 3.4%
- **Assembly** 2.7%
- **Python** 2.0%
- **Other** 3.9%

- DTM with JTAG interface

These are not implemented (yet)

- Trigger module
- Quick access using abstract commands
- Accessing memory using abstract commands
- Authentication

Limitations

- The JTAG clock frequency needs to be lower than the system's clock frequency (see also #163).

Tests

We use OpenOCD's RISC-V compliance tests, our custom testbench in `tb/` and riscv-tests/debug.