48 Debug support (DBG)

48.1 Overview

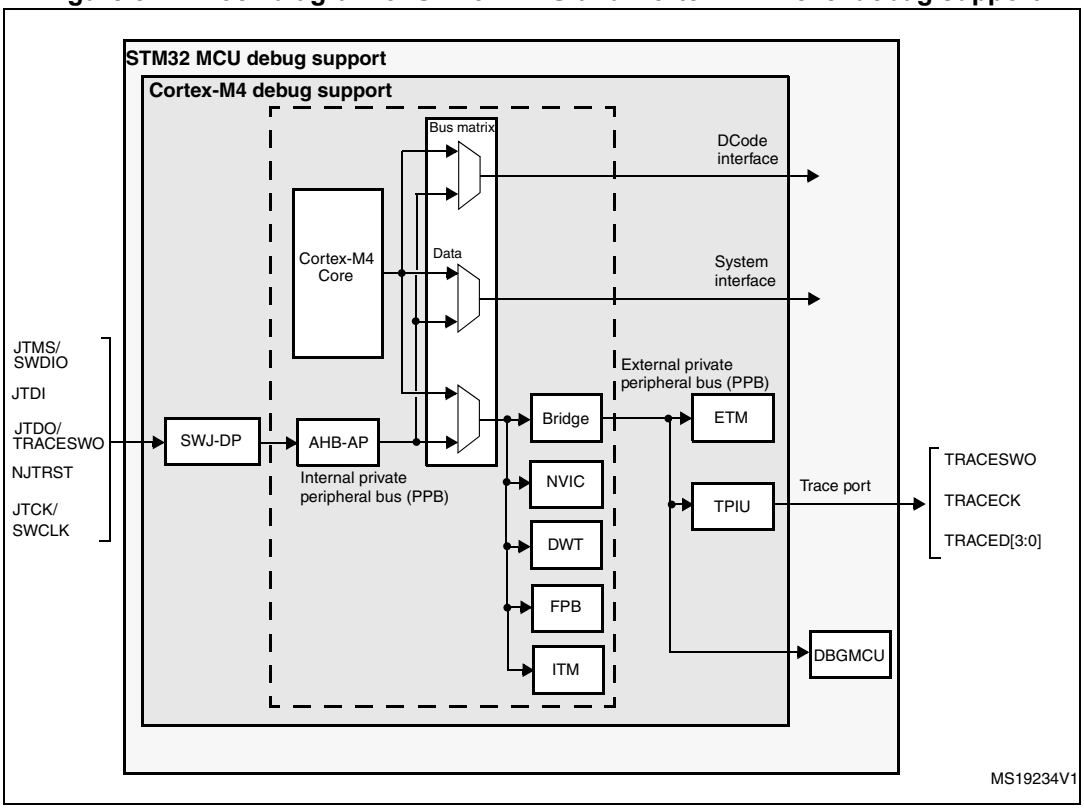
The STM32L4x5/STM32L4x6 devices are built around a Cortex®-M4 core which contains hardware extensions for advanced debugging features. The debug extensions allow the core to be stopped either on a given instruction fetch (breakpoint) or data access (watchpoint). When stopped, the core's internal state and the system's external state may be examined. Once examination is complete, the core and the system may be restored and program execution resumed.

The debug features are used by the debugger host when connecting to and debugging the STM32L4x5/STM32L4x6 MCUs.

Two interfaces for debug are available:

- Serial wire
- JTAG debug port

Figure 542. Block diagram of STM32 MCU and Cortex®-M4-level debug support



Note: The debug features embedded in the Cortex®*-M4 core are a subset of the ARM® CoreSight Design Kit.*