

## 7 General-purpose and alternate-function I/Os (GPIOs and AFIOs)

**Low-density value line devices** are STM32F100xx microcontrollers where the Flash memory density ranges between 16 and 32 Kbytes.

**Medium-density value line devices** are STM32F100xx microcontrollers where the Flash memory density ranges between 64 and 128 Kbytes.

**High-density value line devices** are STM32F100xx microcontrollers where the Flash memory density ranges between 256 and 512 Kbytes.

This section applies to the whole STM32F100xx family, unless otherwise specified.

### 7.1 GPIO functional description

Each of the general-purpose I/O ports has two 32-bit configuration registers (GPIOx\_CRL, GPIOx\_CRH), two 32-bit data registers (GPIOx\_IDR, GPIOx\_ODR), a 32-bit set/reset register (GPIOx\_BSRR), a 16-bit reset register (GPIOx\_BRR) and a 32-bit locking register (GPIOx\_LCKR).

Subject to the specific hardware characteristics of each I/O port listed in the *datasheet*, each port bit of the General Purpose IO (GPIO) Ports, can be individually configured by software in several modes:

- Input floating
- Input pull-up
- Input-pull-down
- Analog
- Output open-drain
- Output push-pull
- Alternate function push-pull
- Alternate function open-drain

Each I/O port bit is freely programmable, however the I/O port registers have to be accessed as 32-bit words (half-word or byte accesses are not allowed). The purpose of the GPIOx\_BSRR and GPIOx\_BRR registers is to allow atomic read/modify accesses to any of the GPIO registers. This way, there is no risk that an IRQ occurs between the read and the modify access.

*Figure 11* shows the basic structure of an I/O Port bit.

Figure 11. Basic structure of a standard I/O port bit

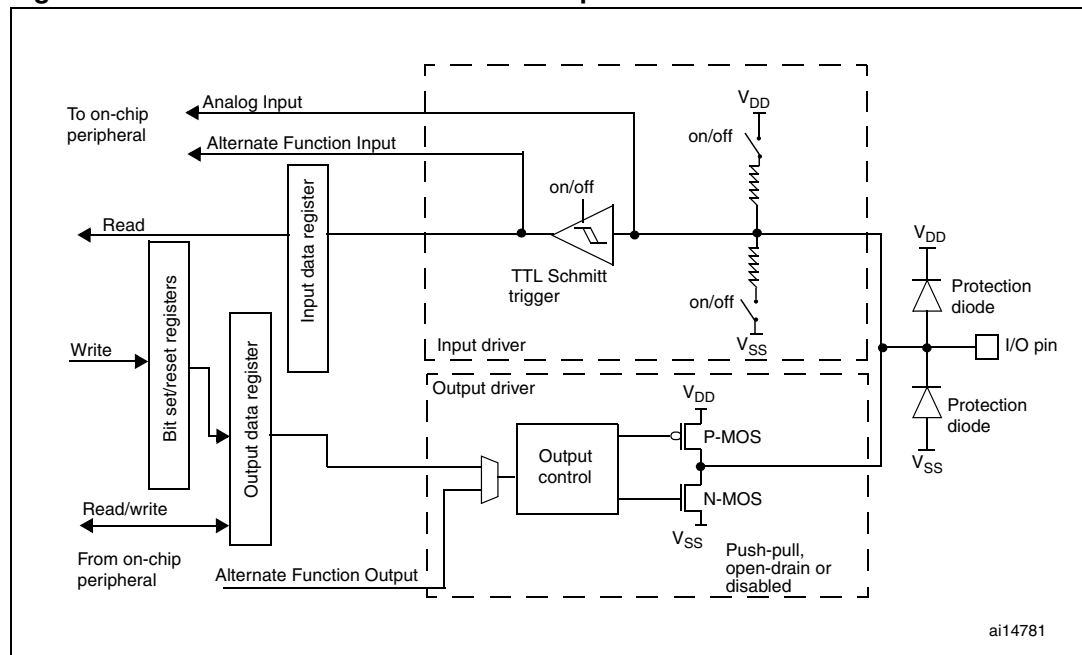
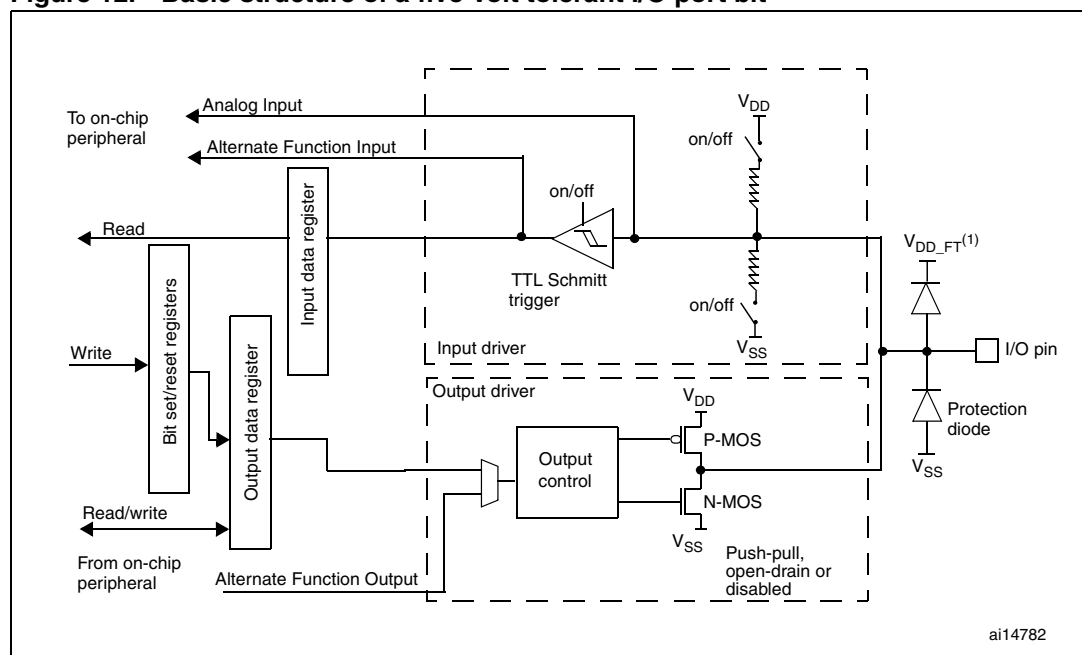


Figure 12. Basic structure of a five-volt tolerant I/O port bit



1.  $V_{DD\_FT}$  is a potential specific to five-volt tolerant I/Os and different from  $V_{DD}$ .