6.3.12 RCC register map

The following table gives the RCC register map and the reset values.

Table 15. RCC register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	RCC_CR	Reserved						PLL RDY	PLL ON	Reserved				CSSON	HSEBYP	HSERDY	HSEON	HSICAL[7:0]								HSITRIM[4:0]					Reserved	HSIRDY	HSION
	Reset value							0	0					0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0		1	1
0x004	RCC_CFGR	Reserved					MCO [2:0]			Reserved		PLLMUL[3:0]				PLLXTPRE	PLLSRC	ADC PRE [1:0]		PPRE2 [2:0]			PPRE1 [2:0]			HPRE[3:0]				SWS [1:0]		SW [1:0]	
	Reset value						0	0	0			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x008	RCC_CIR	Reserved								CSSC	Reserved		PLLRDYC	HSERDYC	HSIRDYC	LSERDYC	LSIRDYC	Reserved			PLLRDYIE	HSERDYIE	HSIRDYIE	LSERDYIE	LSIRDYIE	CSSF	Reserved		PLLRDYF	HSERDYF	HSIRDYF	LSERDYF	LSIRDYF
	Reset value									0			0	0	0	0	0				0	0	0	0	0	0			0	0	0	0	0
0x00C	RCC_APB2RSTR	Reserved													TIM17RST	TIM16RST	TIM15RST	Reserved	USART1RST	Reserved	SPI1RST	TIM1RST	Reserved	ADC1	IOPGRST	IOPFRST	IOPERST	IOPDRST	IOPCRST	IOPBRST	IOPARST	Reserved	AFIORST
	Reset value														0	0	0		0		0	0		0	0	0	0	0	0	0	0		0
0x010	RCC_APB1RSTR	Reserved	CECRST	DACRST	PWRRST	BKPRST	Reserved				I2C2RST	I2C1RST	UART5RST	UART4RST	USART3RST	USART2RST	Reserved	SPI3RST	SPI2RST	Reserved		WWDGRST	Reserved			TIM14RST	TIM13RST	TIM12RST	TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset value			0	0	0					0	0	0	0	0	0		0	0			0				0	0	0	0	0	0	0	0	0
0x014	RCC_AHBENR	Reserved																							FSMCEN	Reserved	CRCEN	Reserved	FLITFEN	Reserved	SRAMEN	DMA2EN	DMA1EN
	Reset value																								0		0		1		1	0	0
0x018	RCC_APB2ENR	Reserved													TIM17EN	TIM16EN	TIM15EN	Reserved	USART1EN	Reserved	SPI1EN	TIM1EN	Reserved	ADC1EN	IOPGEN	IOPFEN	IOPEEN	IOPDEN	IOPCEN	IOPBEN	IOPAEN	Reserved	AFIOEN
	Reset value														0	0	0		0		0	0		0	0	0	0	0	0	0	0		0
0x01C	RCC_APB1ENR	Reserved	CECEN	DACEN	PWREN	BKPEN	Reserved				I2C2EN	I2C1EN	UART5EN	UART4EN	USART3EN	USART2EN	Reserved	SPI3EN	SPI2EN	Reserved		WWDGEN	Reserved			TIM14EN	TIM13EN	TIM12EN	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
	Reset value		0	0	0	0					0	0	0	0	0	0		0	0			0				0	0	0	0	0	0	0	0	0
0x020	RCC_BDCR	Reserved															BDRST	RTCEN	Reserved					RTC SEL [1:0]		Reserved						LSEBYP	LSERDY	LSEON
	Reset value																0	0						0	0							0	0	0
0x024	RCC_CSR	LPWRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	PORRSTF	PINRSTF	Reserved	RMVF	Reserved																						LSIRDY	LSION
	Reset value	0	0	0	0	1	1		0																							0	0
0x02C	RCC_CFGR2	Reserved																													PREDIV1[3:0]		
	Reset value																														0	0	0	0

Refer to *Table 1: Low and medium-density device register boundary addresses* and *Table 2: High-density device register boundary addresses* for the register boundary addresses.