Figure 67. Capture/compare channel 1 main circuit

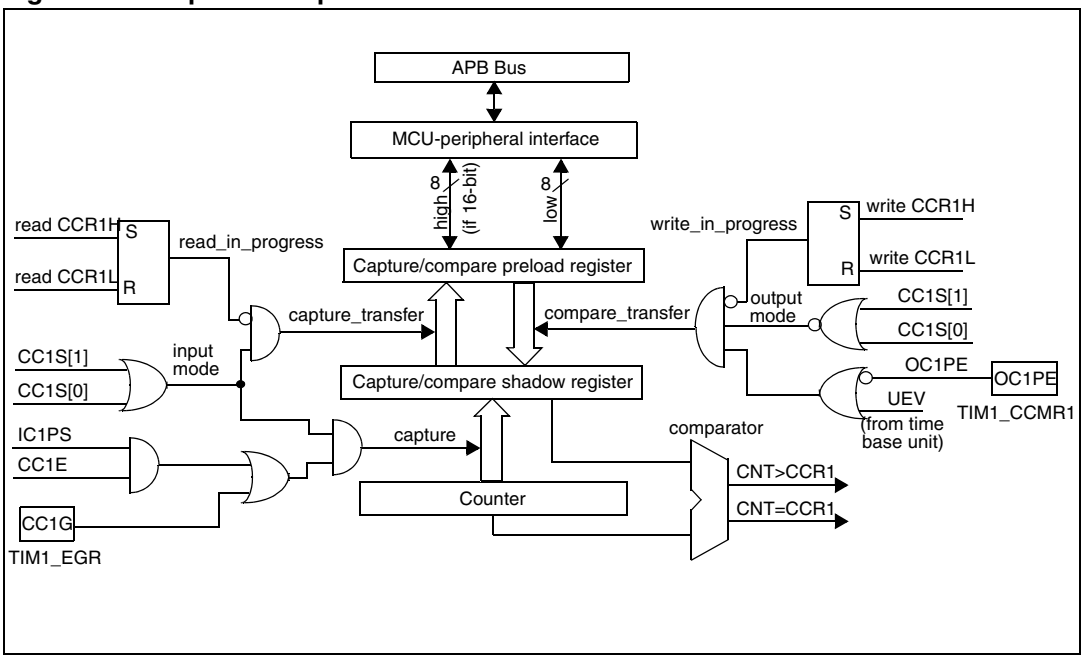

Figure 68. Output stage of capture/compare channel (channel 1 to 3)