Application Note

Introduction to Synchronous DRAM

Manufacturer:	**Maxwell Technologies**
Document Number:	**1004355**
Revision:	**1**
Date:	**April 25, 2003**

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Purpose

This document describes the architecture and features of Maxwell Technologies Synchronous DRAM (SDRAM). A brief discussion of a conventional Dynamic Random Access Memory (DRAM) provides background information on the evolution of the industry standard architecture to the SDRAM.

Abstract

Today's computers, as well as other electronic systems requiring large amounts of memory, utilize DRAM's for main memory. Because of the single transistor cell structure of the DRAM, extremely dense memory arrays can be fabricated in a single device occupying a relatively small footprint.

Conventional DRAM is controlled asynchronously, requiring the system designer to manually insert wait states to meet the specifications of the device. Timing depends on the speed of the DRAM and is independent of the system bus speed. It is these timing limitations that led to the development of the SDRAM.

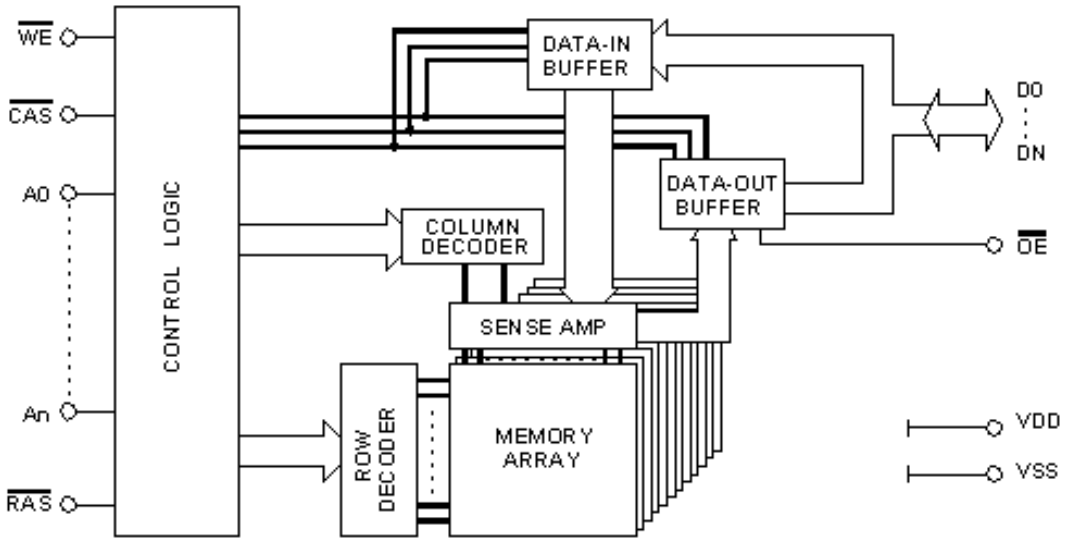
SDRAM is essentially a fast DRAM with a high-speed synchronous interface. I/O's and control signals are synchronized with an external clock, making new options available to the designer. Simplified interface circuitry, as well as high-bandwidth data throughput can be achieved using SDRAM over conventional DRAM.

Conventional DRAM Architecture and Operation

DRAM has been the standard memory component for computer systems since the mid 1970's. Over the years DRAMs have been adopted for virtually all types of systems requiring large amounts of memory. The main advantage DRAM has over other types of memory architectures is the large densities that can be attained due to the fact that the memory cells utilize a single transistor and capacitor; whereas other types of memories are made up of a series of transistors. These densities allow large amounts of memory to be represented by relatively few components. Advances in semiconductor process technology over the years, have allowed DRAM densities to dramatically increase from a few thousand memory cells in the 1970's, to the 256 million cell devices available today.

Although the process technologies for producing DRAMs have made vast improvements, the basic structure has remained the same. DRAMs are rectangular arrays of memory cells, with support logic that is used for reading and writing data into the array and refresh circuitry to maintain integrity of the stored data. The memory array is arranged in rows and columns of memory cells. Each memory cell has a unique location defined by the intersection of a row and column.

Functional Block Diagram of a Conventional DRAM



Conventional DRAM's are asynchronous. Operations in the memory must meet the timing requirements of the device. As long as the control signals are applied in the proper sequence and the timing specifications are met, the DRAM will operate properly. Four logic input signals, along with address inputs, control the operation of the DRAM; Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE), Output Enable (OE) and Addresses A^0 through A^N, where N represents XXX.

- **Row Address Strobe (RAS)** The RAS control input is used to latch the row address and to begin a memory cycle. RAS is required at the beginning of every operation and must remain selected for a predetermined minimum amount of time.

- **Column Address Strobe (CAS)** CAS is used to latch the column address and to initiate the write or read operation. CAS may also be used to trigger a CAS-before-RAS refresh cycle. This refresh cycle requires CAS to remain selected for a predetermined minimum time period. For most memory operations, CAS must remain deselected for a predetermined minimum amount of time.

- **Write Enable (WE)** The WE control input is used to select a read or write operation. The operation performed is determined by the state of the WE when CAS is taken active. It is important that setup and hold timing specifications are met, with respect to CAS, to assure that the correct operation is selected.

- **Output Enable (OE)** During a read operation, OE is set active to assure data does not appear at the I/O's until required. During a write cycle, OE is ignored.

- **Address** The address inputs are used to select memory locations in the array. The address inputs are used to select both the desired row and column addresses.

Reading Data From Memory

To read data from a memory cell, the cell must first be selected by its row and column address. The charge on the cell must be sensed, amplified and sent to the data outputs. With respect to timing, the following sequence is used to read data from a memory cell:

1) The row address is applied to the address inputs for a specified amount of time before RAS goes active (switched from High to Low). RAS must be Low for a minimum amount of time allowing the row latch circuitry to be completed.

2) The column address is applied to the address inputs and held for a specified amount of time before CAS is set active (switched from High to Low). CAS is set Low and held for the specified amount of time.

3) WE is set HIGH for a read operation and must occur before the transition of CAS.

4) CAS must be set active (switched from High to Low), thereby latching in the column address.

5) Data appears at the data output pins after the specified time period.

6) Before a read cycle is considered complete, both RAS and CAS control inputs must be returned to an inactive state (both RAS and CAS set from Low to High).

Writing Data to Memory

To write data to memory, the cell must first be selected by its row and column address and the data to be written must be present at the data inputs. The memory cell is either charged or discharged, depending on whether a 1 or 0 is to be stored. The following sequence is used to write data to a memory cell:

1) The row address is applied to the address inputs for a specified amount of time before RAS is set active. RAS must be held active for a minimum amount of time, allowing the row latch circuitry to be completed.

2) The column address is applied to the address inputs and held for a specified amount of time before CAS is set active. CAS is set active and held for the specified amount of time.

3) WE is set Low for a write operation and must occur before the transition of CAS.

4) CAS must be set Low, thereby latching in the column address.

5) Data must be applied to the data inputs before CAS is set active.

6) Before a read cycle is considered complete, both RAS and CAS control inputs must be returned to an inactive state (both RAS and CAS set from Low to High).

Refreshing the Memory

A DRAM memory cell is basically a capacitor that is charged to produce a 1 or 0. The charge they contain can dissipate over time. When the charge is lost, so is the data within that cell. To prevent this from happening, the DRAM must be periodically refreshed, that is, the charge on the memory cells must be restored. A Read or Write operation must be done to every memory location in the memory array at least one time during the Refresh Rate period, which is typically specified in milliseconds.

There are several different ways to refresh the memory. Three common refresh options are RAS-Only-Refresh (ROR), CAS-Before-RAS Refresh (CBR) and Auto or Self Refresh (SR).

- **RAS-Only-Refresh (ROR)** DRAMs are normally refreshed one row at a time. The refresh cycles are carried out such that all rows are refreshed during the specified refresh period. The following sequence is used to refresh one row of memory cells using RAS-Only-Refresh (ROR):

    1) The row address of the row to be refreshed is applied to the address inputs.

    2) RAS is set to an active state (switched from High to Low). CAS must remain inactive (High).

    3) After the specified amount of time, RAS is set inactive (switched from Low to High).

- **CAS-Before-RAS Refresh (CBR)** When using CAS-Before-RAS Refresh, an internal address counter keeps track of the row address to be refreshed. No row address needs to be specified. The following sequence is used to refresh one row of memory using CBR refresh:

    1) CAS is set active (switched from High to Low).

    2) WE must be in a High state.

    3) After the specified time, RAS is switched from High to Low.

    4) The internal counter determines which row to refresh.

    5) After the required refresh cycle time, CAS is set to a High state.

    6) After the required delay, RAS is set to a High state.

- **Auto Refresh** Auto Refresh, also referred to as Sleep Mode, uses an internal oscillator to establishing the refresh rate and the internal address counter to keep track of the address to be refreshed. To start the Auto Refresh operation, a CBR cycle is initiated, with RAS being held active for the entire time the device is in the sleep mode.

The most difficult aspect of implementing the conventional DRAM into an electronic system is resolving the timing requirements of the device. Because of the asynchronous interface to the conventional DRAM, access time is limited by the timing requirements of the control logic. Interface timing must include wait states to meet the specified setup and hold times of the various memory operations. It is these particular timing limitations which let to the evolution from the conventional DRAM architecture to the Synchronous DRAM (SDRAM) used today.

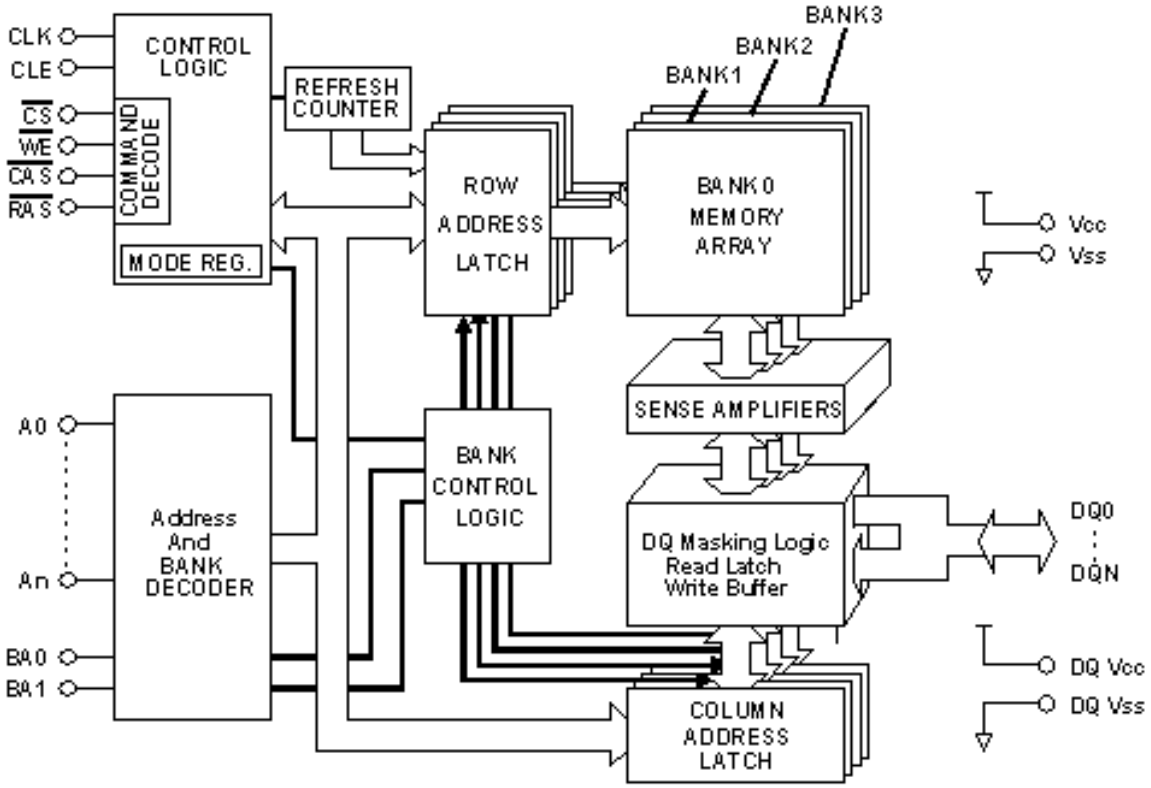
Features of the SDRAM

SDRAM devices were defined by JEDEC to address the performance limitations of older DRAM architectures. The SDRAM devices are capable of faster speeds because, unlike FPM and EDO memory devices, they synchronize memory transactions to the system clock. In older DRAM devices, memory access was executed a certain amount of time after the assertion of control signals, depending on the characteristic propagation delays of the device.

Several factors contribute to greater overall memory bandwidth in SDRAM devices including:

- Fast system clock speeds
- Burst capabilities that allow multiple column accesses for a single read or write row address
- Pre-charging of memory array partitions to reduce reactivation latency

Functional Block Diagram of an SDRAM



Synchronous Dynamic Random Access Memory (SDRAM) is a type of DRAM which operates in synchronization with an external input clock. SDRAM and DRAM have almost identical basic configurations inside the memory, however, since SDRAM's are synchronous with a clock, operations are available that help to achieve higher bandwidth and greatly simplify interface timing. Some operational features of the SDRAM, which are not available in conventional DRAMs, are:

- **Synchronous Control Logic**

  All inputs and outputs are synchronous with the clock. SDRAM's latch each control signal at the transition of the input clock and all input/output data are synchronized with the clock signal. Controls are made easier by synchronizing the memory clock with the system clock.

- **Controls with Commands**

  A command is a combination of the logic levels of control signals. Typical commands include: Activate Command, Read and Write Command, Pre-charge Command, etc. The conventional DRAM is also controlled with control signals, however, it does not have the ability to execute commands.

- **Multiple Bank Architecture**

  The SDRAM memory is separated into several banks, so that the controls can be performed by the bank. For example: since the interleave control can be performed on each bank separately, the pre-charge time is seemingly hidden.

- **Refresh Modes**

  There are two types of refresh operations in the SDRAM: Auto-Refresh and Self-Refresh. The logic state of the CKE control signal determines which refresh operation is used. The Auto Refresh mode uses an internal refresh counter and requires no external addressing. As compared to the Self Refresh mode which is used during periods when the SDRAM is in the low power mode, allowing the SDRAM to refresh its self.

- **Memory and I/O Power Supplies**

  Since large amounts of current are sourced and sunk into the SDRAM during read and write operations, switching noise can be generated which may have an adverse effect on the memory array. Separate power inputs are provided for the I/O signals and the memory array, isolating the memory cells from possible data corruption.

- **Selectable CAS Latency**

  CAS Latency is the number of clock cycles that occur from the input of a command to the output of data. The number of clocks is set in the Mode Register.

- **Selectable Burst Length**

  The burst length is the number of words that can be continuously input/output for a read or write operation.

- **Mode Register**

  The mode register can be set with the CAS latency and burst length. This register retains data until it is rewritten or the device loses power.

SDRAM – Theory of Operation

A significant difference between the conventional DRAM and the SDRAM is the way in which memory access is executed. In a standard DRAM, the toggling of the external control inputs has a direct effect on the internal memory array. Whereas, in a SDRAM, the input signals are latched into a control logic block which functions as the input to a state machine. Therefore, the state machine actually controls the memory access.

Basic operations of the SDRAM, such as Read, Write and Refresh, are initiated by loading control commands into the device. The most common control commands of the SDRAM are:

- Row Address Strobe (RAS)
- Column Address Strobe (CAS)
- Pre Charge
- CAS-before-RAS (CBR) Refresh
- Self Refresh

The Command Set

- **Ignore Command (DELS):** When this command is set (CS = High), the SDRAM ignores command input at the clock. However, the internal status is held.

- **No Operation (NOP):** This command is not an execution command. However, the internal operations continue.

- **Column Address Strobe (CAS) and Read Command:** The CAS command starts a read operation. In addition, the start address of a burst read is determined by the column address and the bank select (BS) address. After the read operation, the output buffer becomes High-Z.

- **Read with Auto-Precharge:** The Read command automatically performs a pre-charge operation after a burst read with a burst length of 1, 2, 4, or 8.

- **Column Address Strobe (CAS) and Write Command:** This command starts a write operation. When the burst write mode is selected, the column address and the bank select address becomes the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address and bank select address.

- **Write with Auto-Precharge:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4, or 8, or after a single write operation.

- **Row Address Strobe (RAS) and Bank Activate:** This command activates the bank that is selected and determines the row address.

- **Precharge Select Bank (PRE):** This command starts a precharge operation on the bank selected.

- **Refresh (REF/SELF):** This REF/SELF command starts the refresh operation. There are two types of refresh operations which can be carried out with the REF/SELF command: auto-refresh, and self-refresh.

- **Mode Register Set (MRS):** The SDRAM has a mode register which is programmed by the user to select the read latency, burst length, and burst type used during read/write operations. After the power-up sequence, the MRS command must be issued to initialize the device. This command is issued by setting the RAS, CAS, CS and WE control inputs Low prior to the positive edge of the clock. The data to be loaded into the Mode Register is applied to the address pins. During the MRS cycle, no other command can be issued. If it is necessary to modify the functionality of the device, it can be altered by re-programming the Mode Register with a MRS command.

Functional Operations

- **POWER UP SEQUENCE** SDRAM must be initialized with the correct power-up sequence:

    1) Apply power and start clock. Attempt to maintain a NOP condition at the inputs
    2) Maintain stable power, stable clock, and a NOP condition for the specified minimum time period
    3) Issue precharge commands for all banks of the device
    4) Issue 8 or more auto-refresh commands
    5) Issue a mode register set command to initialize the mode register

- **PRECHARGE (PRE)** This command is used to precharge a bank selected by bank control inputs. The precharge command is initiated by activating CS, RAS, WE and selecting the bank.

- **I/O Control - DQMU/DQML** The SDRAM can mask input/output data by means of DQMU/DQML. DQMU masks the upper byte and DQML masks the lower byte. During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, thus enabling data output. When DQMU/DQML is set High, the output buffer becomes High-Z, disabling data output. During writing, data is written by setting DQMU/DQML

to Low. When DQMU/DQML is set to High, the previous data is held (new data is not written).

- **READ** The Read command is optimized for single read accesses. When the Read command is executed, data is available a set number of clocks later, as defined by the CAS latency mode in the mode register. Latencies of 2 and 3 cycles are supported. Another Read command can be executed while the current Read command is in progress, causing the state machine to transition so that a new row address can be processed. Any read or write command can be terminated by another read or write command to an active Row. Only one row in a bank can be active at a time. In all cases, timing constraints cannot be violated. When following a read with a write, it is required to set DQM high for 1 cycle. This is not typically a problem since the delay from DQM to Data out is 2 clock cycles. It is possible to have read data followed by write data in back-to-back clock cycles.

- **WRITE** Write cycles can be either single transfers or burst transfer. Execution of a Read command while the write operation is in progress causes the write operation to be terminated and the read operation to begin. Unlike the Read operation, where a subsequent Read command is allowed as long as it is to the opposite bank, execution of a subsequent Write command while the write operation is in progress causes the operation to be terminated and a new write operation to begin.

- **AUTO REFRESH** This command is similar to a CAS-Before-RAS refresh command in asynchronous DRAMs. The auto refresh command is initiated by activating CS, CAS, WE and deactivating RAS on the same clock rising edge. One Auto Refresh cycle refreshes one row selected by the on-chip refresh counter. The refresh counter is incremented one step during each Auto Refresh cycle. Once an Auto Refresh cycle has been invoked, it is controlled internally until its duration. NOP cycles must be inserted during the entire Auto Refresh cycle time. Since the SDRAM is a dynamic memory device, the stored data must be refreshed periodically or it will be lost. To avoid data loss, all rows in all banks must be refreshed during the maximum refresh interval specified.

- **SELF REFRESH** The SDRAM features an on-chip refresh cycle timing generator which can be used in conjunction with the row refresh counter to completely refresh the banks of DRAM under internal control. Once this command is invoked, the cycle timing generator performs a burst refresh sequence. Self refresh can be invoked only when all banks of the device are idle. While the device is in self refresh mode, CKE is the only enabled input to the device. All other inputs, including the clock, are disabled and ignored.

Conclusion

The DRAM has been the memory architecture used in computer systems, and other electronic systems requiring large amounts of memory, since the mid-1970's. Conventional DRAM's are asynchronous, with memory access being controlled by logic inputs and timing

set manually by the user. Memory access times are greatly limited by the timing specifications of the device. As processing speeds increased, conventional DRAM access times became the limiting factor in overall system performance. Slow access times of conventional DRAM's led to the evolution and industry standard architecture of the Synchronous DRAM. Although the memory cell structure has remained the same, the interface to the device has been enhanced to significantly increase access times. Through the use of clocked inputs, read/write operations using a burst mode, and a multiple bank architecture, memory access time has greatly reduced. The SDRAM is now the memory architecture of choice for main memory.

Glossary of Terms

Access Time	Access time is the time from the start of one device access to the time when the next access can be started.
Array	The area of a memory device that stores the data. The array consists of rows and columns, where each memory cell is located at an address where an intersection occurs. Each bit in memory is found by its row and column coordinates
Asynchronous	A process where operations proceed independently.
Auto Precharge	An SDRAM function that closes a page at the end of a burst operation.
Auto Refresh	A mode where an internal oscillator establishes the refresh rate and an internal counter keeps track of the address to be refreshed.
Bank	A bank can mean the number of physical banks (same as Rows) on the SDRAM module. It can also mean the number of internal logical banks (usually 4 banks nowadays) within an individual SDRAM device.
Burst Mode	Bursting is a rapid transfer of data to a series of memory cell locations.
Bus Cycle	A single transaction between a memory device and the system CPU.
CAS	Column Address Strobe – A control signal that latches a column address into the SDRAM control register.
CAS-Before-RAS (CBR)	Column address strobe before row address strobe. CBR is a fast refresh function that keeps track of the next row to be refreshed.
Column	Part of the memory array. A bit is stored where a row and column intersect.
DQM	Data mask signal used for masking during a write cycle. There is one DQM signal per eight I/Os.

DRAM	Dynamic Random Access Memory – A type of memory device usually used for mass storage in computer systems. The term Dynamic refers to the constant refresh the memory must have to retain data.
FPM	Fast Page Mode – A common SDRAM data access scheme.
Interleaving	The process of read/writing data alternately from two or more pages in the SDRAM.
JEDEC	Joint Electron Device Engineering Council
Latency	The length of time, usually expressed in clock cycles, from when a request to read a memory location has occurred and when the data is actually ready.
Memory Cycle Time	The time it takes for a complete memory operation to take place, such as a read or write.
Page	The number of bytes that can be accessed with one row address.
Page Mode	Page Mode is an operation that takes place when RAS is taken logic low and a column address is strobed in. The SDRAM remembers the last row address and stays on that row and moves to the new column address.
RAS	Row Address Strobe – The control signal that latches the row address into the SDRAM. It is used in conjunction with the column address to select an individual memory location.
RAS to CAS Delay	The time between Row Access Strobe to Column Address Strobe.
Read Time	The time required for data to appear at the output once the row and column address become valid. Read Time is also referred to as Access Time.
Refresh	A periodic restoration of an SDRAM cell charge which is needed to maintain data.
Refresh Cycle	The time period in which one row of an SDRAM is refreshed

Refresh Period	The minimum time that each row in the SDRAM must be refreshed
Row	Part of the memory array. A bit is stored where a row and column intersect.
Strobe	An input control signal that latches data synchronously into the SDRAM
Synchronous Memory	A memory device that has its signals synchronized to a reference clock.
Write Time	The time from which data is latched into the SDRAM until it is actually stored in a memory location.