What's All This Flash Stuff?

National Semiconductor
Application Note 920
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INTRODUCTION

Flash technology is basically an outgrowth of EPROM technology. Toshiba first invented Flash technology in the mid 80's. Intel quickly developed its own version based on a simpler cell structure, ETOX (EPROM Tunnel Oxide). Cells based on the ETOX structure are the basis for the majority of the Flash products sold today.

Flash memory takes the features of EEPROM and combines them with the density of EPROM *(Figure 1)*. Like EEPROM, Flash offers in-circuit programmability. But Flash also uses only one transistor per cell which enables it to achieve densities as high as 16Mb. This is equivalent to current DRAM densities. In fact, Flash should keep pace with and possibly exceed DRAM densities because there is no additional capacitor in the cell.

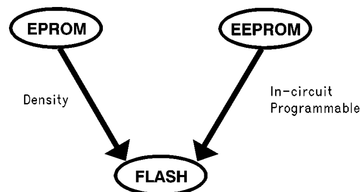

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FIGURE 1. FLASH Advantage

There are actually two different kinds of Flash memory. One kind, NOR Flash, is very similar to EPROM's. The other, called NAND Flash, is comparable to E^2PROM's. The main difference between NOR and NAND is how the cells are programmed/erased and how data is read off the device. National Semiconductor is the only U.S. manufacturer to offer both types of Flash. In the NOR Flash, National offers the 1Mb NM28F010 and the 4Mb NM28F040. For NAND, National offers the 16Mb NM29N16.

PROGRAM/ERASE METHODS

Both types of Flash have their own advantages and disadvantages due to the program/erase method used and the architecture. NOR Flash uses EPROM programming methods but erases using an E^2PROM method. For programming, NOR uses Hot Electron-Injection (HEI). In this operation, the control gate is held at V_{PP} (12V) while the drain is at 6V and the source grounded *(Figure 2)*. Electrons are injected from the drain to the floating gate. This operation requires a lot of current (mA's) and is the reason why EPROMs and NOR Flash require a 12V supply. The advantage of this method is a relatively fast program (10 μs/byte) while also offering individual byte programmability. For erase, NOR uses Fowler-Nordheim (F-N) tunneling like E^2PROMs. To prevent over erasure, an additional step has been added to the erase operation. Prior to erasing, all bytes are programmed to the "1" state. They are then erased by putting the control gate at ground and the source at 12V. Electrons tunnel from the floating gate to the source. The added step to prevent overerasure causes NOR Flash to take longer to erase ($\approx$1 sec.).

An obstacle to the system designer is that individual bytes can not be erased, whole blocks must be erased. National's NM28F040 offers one the smallest block sizes at 16 Kb. The 1Mb parts (xx28F010) have standardized on the entire chip erasing at the same time.

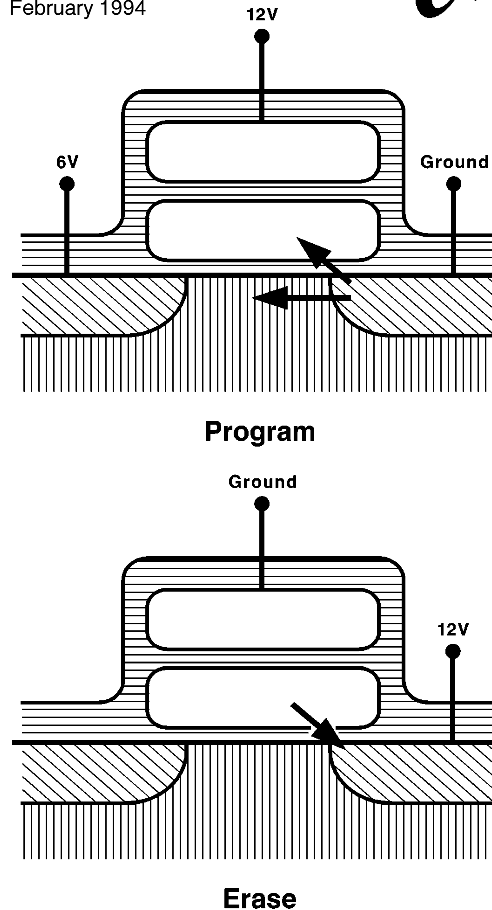

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FIGURE 2. NOR Program/Erase

In contrast to NOR Flash, NAND Flash uses F-N tunneling for both program and erase operations. Programming the cell involves placing the control gate at V_{PP} ($\approx$ 20V) while the channel region is grounded *(Figure 3)*. Electrons tunnel through the gate oxide into the floating gate. An advantage of this method over HEI is that less current is used (μA's). Since the tunneling is from the channel, there is also less stress on the gate oxide. The lower current used allows NAND devices to be built with a single 5V power supply. The lower stress gives NAND devices higher endurance levels (10^6 program/erase cycles versus 10^5 for NOR Flash).

Erasing the NAND cell involves grounding the control gate and pulling the channel region to V_{PP} ($\approx$ 20V). Without the added erase step used by NOR devices, NAND is able to erase in milliseconds rather than seconds.

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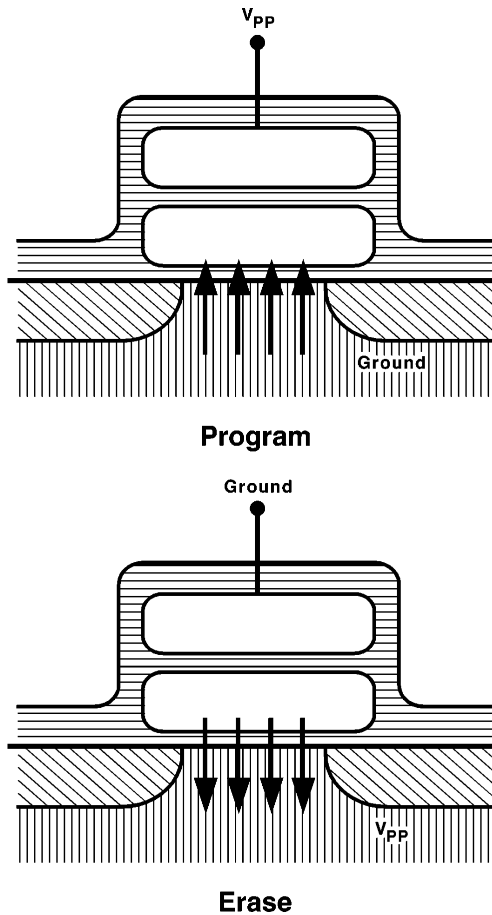

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FIGURE 3. NAND Program/Erase

FLASH INTERFACING

Interfacing to a NOR Flash device is just like interfacing to an EPROM. In fact, some NOR Flash devices maintain the same pinout configuration as the similar density EPROM *(Figure 4)*. Reads are performed by placing the address on the address lines, pulling $\overline{CE}$ and $\overline{OE}$ low and then reading the databus.

Programming involves sending in a programming command (40H, this and the following NOR command examples are standardized commands for 1Mb devices) while strobing $\overline{WE}$ low. This is followed by the address and the data while again strobing $\overline{WE}$ low. A successful program can be verified by issuing a program verify command (C0H) and reading the data. The data read out then needs to be compared against the data inputted by the processor.

The erase operation involves writing two consecutive erase commands (20H). Again a verify command (A0H) is sent to check for a successful erase. There is typically a one second delay between the second erase command and the erase verify command.

Interfacing to a NAND device is similar to interfacing to a peripheral device on a PC motherboard. The device does not have any address pins but instead has eight I/O lines

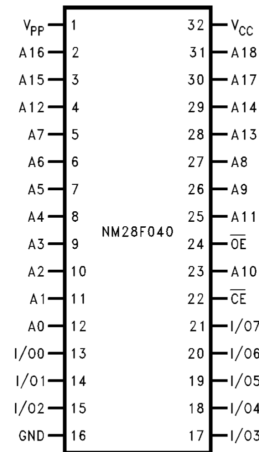

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FIGURE 4. NM28F040 Pinout

through which all data and commands pass *(Figure 5)*. Because of this architecture, a NAND device does not map into the system memory byte for byte. In fact, as little as three bytes of the system memory-map can be used to address 2 MBytes in a single NAND device. Data is pulled out of the NAND device in pages. Pages are 256 bytes with the NM29N16 providing an additional 8 bytes for a total of 264 bytes per page. The additional eight bytes may be used for redundancy or error code correction. The read operation involves sending the read command (00H) followed by a three cycle address. The address tells the device which page (16 pages to a block, 512 blocks to a device) to pull from the array and where to set the pointer within the page. The data is pulled from the array and is ready to read after

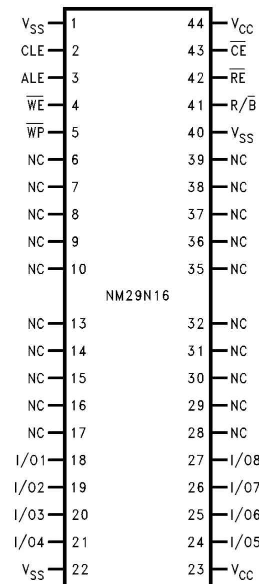

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FIGURE 5. NM29N16 Pinout

a 25 μs delay. Sending consecutive $\overline{RE}$ pulses reads out data a byte at a time starting at the location pointed to by the pointer.

Programming the device involves sending the data input command (80H), the three cycle address and the data, a byte at a time. This is followed by the program command (10H).

The ready/busy (R/$\overline{B}$) pin will go low for approximately 300 μs while the programming occurs. A verify command (70H) can be sent to ensure of proper operation.

The erase operation consists of sending in the auto block erase command (60H) followed by a two cycle address of the block to erase. The NM29N16 offers designers increased flexibility by using one of the smallest block sizes of any Flash at 4 KBytes. The erase execution command (D0H) is then given to commence the erase procedure. Again, the ready/busy (R/$\overline{B}$) pin will go low, this time for approximately 6 ms. The verify command can again be used to check for proper operation.

SUMMARY

Overall, Flash memory is a step closer towards the ideal memory device that includes non-volatility with fast read times, high density and low cost. There are a number of compromises that the system designer must make in using Flash, but these are more than overcome by the benefits enjoyed by using Flash (just think of trying to pull an EPROM from a system already in the field as opposed to sending the customer a disk to update his system). In the future, Flash will also allow new systems to come to market that otherwise would not be able to because of weight, cost or power constraints.

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