Micron® *e*-MMC™ Embedded Memory Simplifies High-Capacity Storage for Mobile and Embedded Systems

Summary

This white paper addresses the various functions NAND designers face today. It also discusses the ways that *e*-MMC embedded memory can provide the necessary NAND Flash functions in an easy-to-use BGA package, saving significant resources that would otherwise go to hardware and software development.

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Overview

Consumer-class, mobile product designers are constantly looking for high-capacity storage to enable their products to store more pictures, movies, MP3s, or simple data files. NAND Flash memory continues to meet these demands with single-level cell (SLC) and multi-level cell (MLC) technologies.

For designs using mid-range densities, SLC NAND Flash will continue to be a good choice. Current SLC NAND Flash devices require only single-bit error correction code (ECC) per 512 bytes. As SLC NAND Flash geometries shrink, it is anticipated that ECC requirements for these devices will only increase slightly. Next-generation wireless and embedded processors will include more sophisticated ECC capabilities, providing direct support for future SLC NAND Flash memory devices.

New application requirements present obvious design challenges for embedded system designers and processor manufacturers.

Current MLC devices require 4 bits of ECC for each 512-byte sector. With future generations of MLC NAND Flash, ECC requirements are expected to exceed 8-bit correction for each 512-byte sector. These types of advanced ECC circuits are implemented in the NAND Flash controller hardware within the processor, so care must be taken to ensure that the processor supports the ECC requirements of the NAND Flash device.

Added to this consideration is the need for an efficient interface between the processor and the NAND Flash device. Designers can smooth implementation by selecting an interface that is supported by many processors.

Rapidly changing requirements present obvious design challenges for embedded system designers and processor manufacturers. In addition to hardware ECC requirements, there are planned architectural changes to improve performance in MLC NAND—such as increasing the page size from 2K bytes to 4K bytes and options for dual-plane arrays—which will mandate other changes as well. To keep pace with NAND Flash manufacturers, system designers and processor manufacturers will need to allocate additional resources for hardware and software development, which could prove to be a significant challenge in itself.

Open NAND Flash Interface (ONFI) Standard

To minimize the impact of competing and sometimes incompatible NAND Flash architectures, Micron and several other NAND Flash suppliers, controller manufacturers, and designers have joined together to announce the Open NAND Flash Interface (ONFI) standard. The primary goal of the ONFI standard is to increase compatibility and make the embedded system designers' job easier. That said, it does not diminish the importance of embedded processor vendors staying abreast of NAND Flash development.

A Simpler Approach

Processors that provide direct NAND Flash support will typically yield the lowest bill-of- materials (BOM) cost. However, abstracting the complexities of NAND Flash operations insulates designers from concerns relative to technology changes as high-density NAND Flash evolves. Additional benefits include potentially shorter development cycles and reduced resource allocations.

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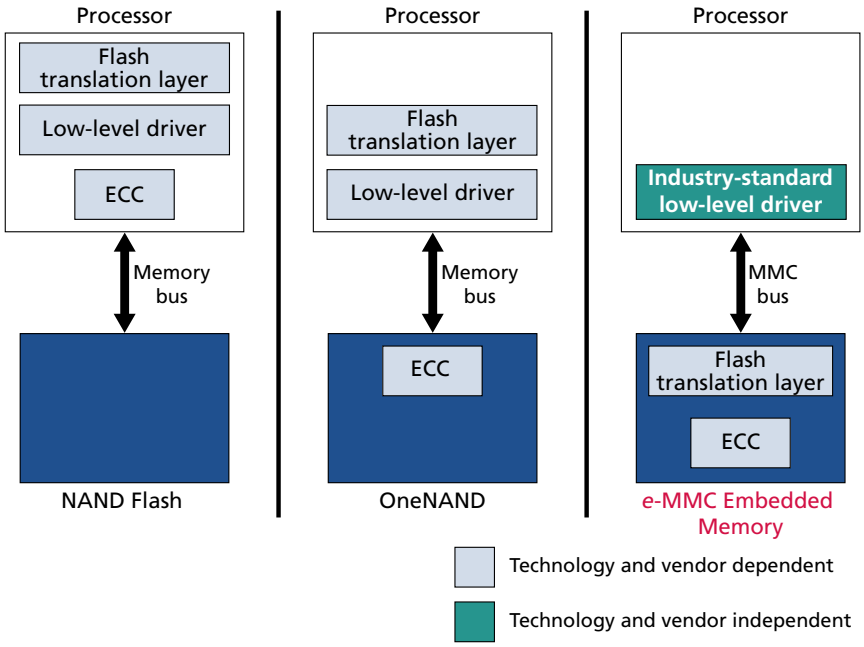
In concept, the evolution of NAND Flash is similar to the evolution of personal computer hard drives when they were introduced and the ATA specification was established. Providing a high-level, abstracted interface enables the processor and software to treat NAND Flash devices like simple, block-oriented file systems. It also enables NAND Flash management tasks, such as error correction, bad block management, and wear leveling, to be incorporated.

Traditional Solutions

While several NAND Flash suppliers have attempted to solve various aspects of the embedded processor challenge, few have used an abstracted implementation with a standard interface. The figure below shows a comparison of three currently offered solutions. The configuration on the left shows a processor that supports a direct NAND Flash interface. This implementation provides the lowest cost and relies exclusively on the wireless processor for ECC support. Block management and wear leveling are typically handled by software running on the processor.

NAND Flash Configurations



SLC NAND Flash requires a minimum of 1-bit ECC. While these relatively simple ECC algorithms can be implemented in software, higher-performance applications will require hardware assistance. MLC NAND Flash currently requires a minimum of 4-bit ECC. Future devices will require more complex ECC and block management and will continue to escalate the demands on processor-supporting hardware.

The configuration in the center of the figure shows the interesting approach Samsung has taken with their OneNAND offering, targeting processors that include a NOR-like interface rather than a direct NAND Flash interface. This approach is attractive for low-density designs, but becomes cost-prohibitive when die are stacked to achieve higher densities. Because each die has roughly 5 percent allocated for the interface, providing multiple die in a single package would only be possible at a significant premium.

Samsung has also chosen to integrate 1-bit ECC hardware on the die. This addresses the ECC challenge, but leaves block management and driver software to the wireless processor.

The configuration to the right in the figure shows the abstracted implementation used in Micron's *e*-MMC™ embedded memory. A single controller is packaged in a BGA with one or more NAND Flash devices. With NAND Flash managed by the controller, the necessary

software support can be provided by a simple, low-level driver. Managing several NAND Flash devices with a single controller is also a cost-effective approach for any density; the first product offered by Micron will be a 1-gigabyte device.

Abstracted Solutions

Some NAND Flash vendors already offer abstracted implementations. The iNAND™ from SanDisk includes a secure digital (SD) interface; *e*-MMC embedded memory from Micron uses an industry-standard MultiMediaCard (MMC) interface. Virtually all wireless processors include SD or MMC interfaces.

The table below shows a comparison of the iNAND and *e*-MMC embedded memory offerings.

Abstracted Implementations

Features	iNAND	*e*-MMC
BGA package size (mm)	12 x 18 x 1.2	12 x 16 x 1.2
Maximum clock speed	25 MHz	52 MHz
Maximum bandwidth	12.5 MB/s	52 MB/s
Data bus width (bits)	1 4	1 4 8
Total number of signals	3 6	3 6 10
Power supply	3.3V only	1.8V / 3.3V1
Memory density	Up to 4GB	Up to 8GB
Future DRAM offering	?	Planned
Flash technology independent	Yes	Yes
Bus standard	SD	MMC

The processor interface can support 1.8V or 3.3V operation. A separate 3.3V supply is used for the NAND Flash devices.

In addition to eliminating NAND Flash dependencies, such as SLC/MLC or varying page sizes, these new technologies offload block management and wear-leveling tasks from the operating software to the controller. Depending on the NAND Flash support provided by the software, this can potentially save valuable execution time and code-storage space.

With a standard, high-performance MMC interface, *e*-MMC embedded memory supports up to 52 megabytes per second (peak) using an 8-bit data bus. Additionally, the single-controller die can be packaged with a variety of NAND Flash components. The common interface, BGA pinout, and package design provide a consistent implementation over a range of densities.

A less obvious benefit of *e*-MMC embedded memory is the ongoing support plan for various NAND Flash densities. Because the interface to the processor does not change, the underlying NAND Flash technology inside the BGA can change and evolve without impacting the application. This approach extends the longevity of higher-density solutions and makes it possible to support multiple densities with a single printed circuit board (PCB).

e-MMC embedded memory includes a standard block-level interface and an error-management and wear-leveling controller, freeing the processor from these tasks. This functionality alone could eliminate the need for a higher-performance processor or additional hardware/software design resources. The *e*-MMC embedded memory controller is optimized to take advantage of specific NAND Flash performance features, including program caching and read caching. This can provide a significant performance improvement over other implementations. It is also possible to boot directly from *e*-MMC, as detailed in Micron's Technical Note TN-29-18, "Booting from Embedded MMC," available at micron.com/products/nand/technotes.

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Conclusion

For designs requiring low- or medium-density NAND Flash, SLC NAND Flash will continue to be a good choice. For higher-density designs, several processors already support the necessary ECC for today's MLC NAND Flash and future SLC NAND Flash devices. The challenge for next-generation embedded processor designers is to meet the increasing ECC support requirements of future MLC NAND Flash devices.

The ONFI standard should help minimize the differences among NAND Flash devices from different vendors. However, hardware development to support even these ONFI-compatible devices will still reside with processor manufacturers. The software development required to support all direct-access NAND Flash devices will keep third-party software vendors, developers, and system integration groups busy.

Processor manufacturers that provide ongoing support for direct NAND Flash will typically provide the lowest overall pricing. For manufacturers that elect not to support future NAND requirements, or whose road maps do not align directly with those of NAND Flash suppliers, *e*-MMC embedded memory offers an attractive solution.

Micron's abstracted solution provides all of the necessary NAND Flash functions in an easy-to-use BGA package, saving significant resources that would otherwise go to hardware and software development. In addition to providing all these essential features, Micron *e*-MMC embedded memory offers higher performance by removing the burden of several low-level tasks from the processor.

About Micron

Micron Technology, one of the world's most efficient and innovative semiconductor companies, manufactures and markets a full line of DRAM components and modules, NAND Flash memory, and other semiconductors. Our broad product line includes both legacy and leading-edge solutions, offered in multiple generations, densities, configurations, and packages to meet the diverse needs of our customers. With operations in 18 countries, customers can count on us to deliver the expert design, manufacturing, sales, and technical support—and ultimately, the high-performance, advanced semiconductor solutions—that go into successful product designs.