Embedded MultiMediaCard
8GB
(*e*•MMC™)

Datasheet
Ver 1.1

Sep 2011

Table of Contents

KE44B-26BN/8GB

8Gbytes 1.8V/3.3V Dual Supply.

Product Features :

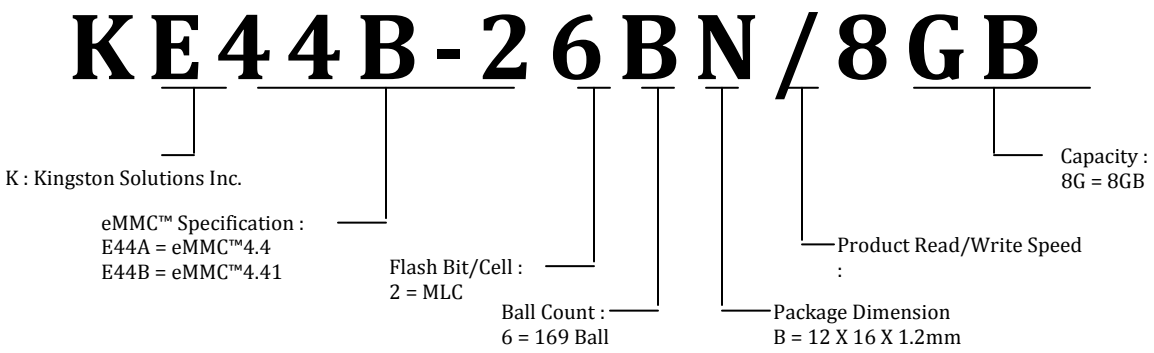
- Packaged NAND flash memory with *e*•MMC™ 4.41 interface
- 8 Gbytes of data storage
- Compliant with *e*•MMC™ Specification Ver 4.41
- Full backward compatibility with previous *e*•MMC™ Ver4.3 system specification
- Bus mode
  - High-speed MultiMediaCard protocol
  - Provide variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52MHz(high Speed)
  - Support three different data bus widths : 1 bit, 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
- Support (Alternate) Boot Operation Mode to provide a simple boot sequence method
- Host initiated explicit sleep mode for power saving
- Enhanced Write Protection with Permanent and Partial protection options
- Support Background Operations & High Priority Interrupt (HPI)
- Support enhanced storage media feature for better reliability
- Operating voltage range :
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- Operating temperature range: –25°C to +85°C
- System Performance
  - Multiple block read (x8 at 52MHz) : up to 28Mbyte/s
  - Multiple block write (x8 at 52MHz) : up to 14Mbyte/s
- Package :
  - 12mm x 16mm x 1.2mm
- Weight :
  - 364mg (8GB)

- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure erase, secure trim and secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options

Device Summary

Product Part number	Density	Package	Operating voltage
KE44B-26BN/8GB	8GB	FBGA169	VCC=3.3V, VCCQ=1.8V/3.3V
-	-	-	

Ordering Information



1. Product Description

The KE44B-26BN/8GB is an embedded flash memory storage solution with MultiMediaCard™ interface (*e*•MMC™). The *e*•MMC™ was developed for universal low-cost data storage and communication media. The KE44B-26BN/8GB is fully compatible with MMC bus and hosts. Empowered with a new *e*•MMC™ 4.41 feature set such as Boot and RPMB partitions, HPI, Background Operations and HW Reset the KE44B-26BN/8GB *e*•MMC™ is the optimal device for reliable code and data storage.

The KE44B-26BN/8GB uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by embedded flash management software running as firmware on the flash controller , which an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

The KE44B-26BN/8GB makes available to the host sudden power failure safe-update operations for the data content, by supporting reliable write features.

The KE44B-26BN/8GB is an universal low cost data storage and communication media. It is designed to cover a wide area of applications as smart phones, cameras, organizers, PDAs, digital recorders, MP3 players, pagers, electronic toys, etc. Targeted features are high mobility and high performance at a low cost price. These features include low power consumption and high data throughput at the memory card inter-face.

1.1. *e*•MMC™ Standard Specification

The KE44B-26BN/8GB device is fully compatible with the JEDEC Standard Specification No. JESD84-A4411. This datasheet describes the key and specific features of the KE44B-26BN/8GB device. Any additional information required to interface the device to a host system and all the practical methods for card detection and access can be found in the proper sections of the JEDEC Standard Specification.

2. Product specification

2.1. System performance

System performance	Typical value		Unit
	KE44B-26BN/8GB	-	MB/s
Multiple block read sequential	28	-	MB/s
Multiple block write sequential	14	-	MB/s

Note : Values given for an 8-bit bus width, a clock frequency of 52MHz, VCC=3.3V and VCCQ=3.3V.

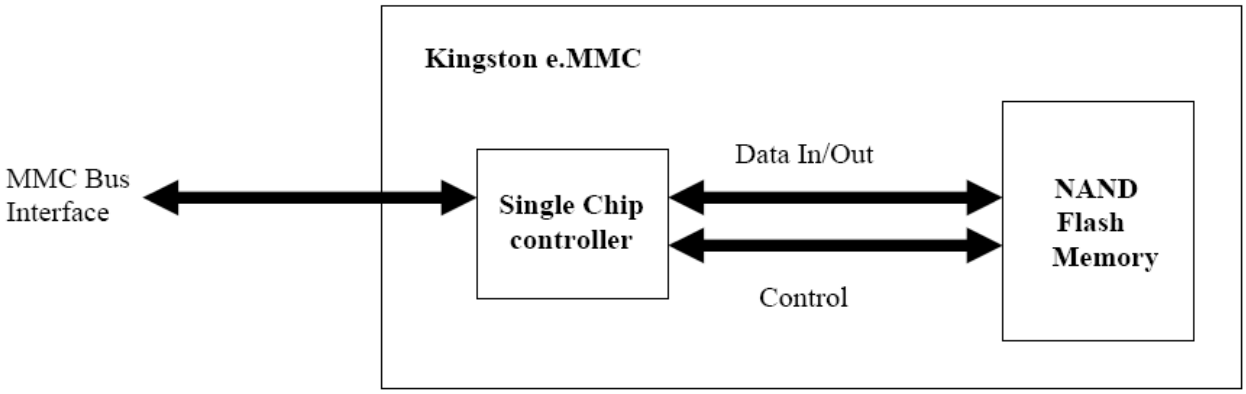
Operation	Test conditions	Current consumption				Unit
		KE44B-26BN/8GB		-		
		Typ	Max	Typ	Max	
Read	VCC= 3.3V±5% VCCQ=3.3V±5%	50	TBD	-	-	mA
Write		70	TBD	-	-	
Stanby		120	TBD	-	-	uA

Note : Values given for an 8-bit bus width, a clock frequency of 52MHz.

3. Device physical description

The KE44B-26BN/8GB device contains a single chip MMC controller and NAND flash memory module, see below : Device block diagram.
The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

***e*•MMC™ I/F Block Diagram**



4. MMC interface

4.1. Signals description

4.1.1. Clock (CLK)

The Clock input, CLK, is used to synchronize the memory to the host during command and data transfers. Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

4.1.2. Command (CMD)

This signal is a bidirectional command channel used for card initialization and transfer of com-mands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the MultiMediaCard bus master to the card and responses are sent from the card to the host.

4.1.3. Input/outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the card or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the MultiMediaCard controller. The MultiMediaCard includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the card disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the card disconnects the internal pull-ups of lines DAT1–DAT7.

4.1.4. VCC core supply voltage

VCC provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase). The core voltage (VCC) can be within 2.7V and 3.6V.

4.1.5. VSS ground

Ground, VSS, is the reference for the power supply. It must be connected to the system ground.

4.1.6. VCCQ input/output supply voltage

VCCQ provides the power supply to the I/O pins and enables all outputs to be powered independently from VCC. The input/output voltage (VCCQ) can be either within 1.65V and 1.95V (low voltage range) or 2.7V and 3.6V (high voltage range).

4.1.7. VSSQ supply voltage

VSSQ ground is the reference for the input/output circuitry driven by VCCQ.

MultiMediaCard interface pin configuration

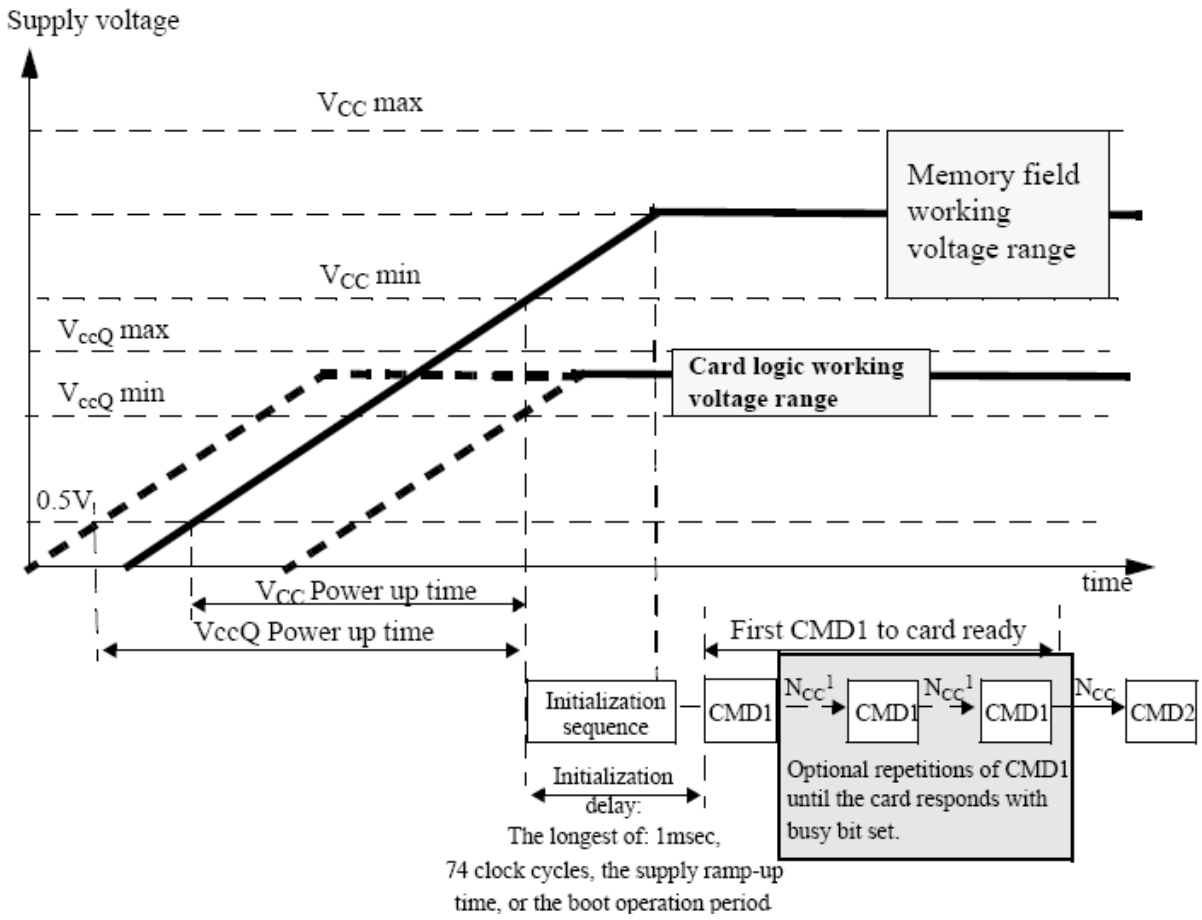
Name	Type[1]	Description
CLK	I	Clock
DAT0[2]	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
V_{CC}	S	Supply voltage for Core (BGA)
$V_{CC}Q$	S	Supply voltage for I/O (BGA)
V_{DD}	S	Supply voltage (card)
V_{SS}	S	Supply voltage ground for Core (BGA)
V_{SS1}	S	Supply voltage ground (card)
V_{SS2}	S	Supply voltage ground (card)
$V_{SS}Q$	S	Supply voltage ground for I/O (BGA)
NOTE 1 I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply. NOTE 2 The DAT0–DAT7 lines for read-only cards are output only.		

4.2. Bus Concept

The KE44B-26BN/8GB device supports the MMC protocol. For more details, refer to section 6.4 of the JEDEC Standard Specification No. JESD84-A441. The section 12 of the JEDEC Standard Specification contains a bus circuitry diagram for reference.

4.3. Power-up

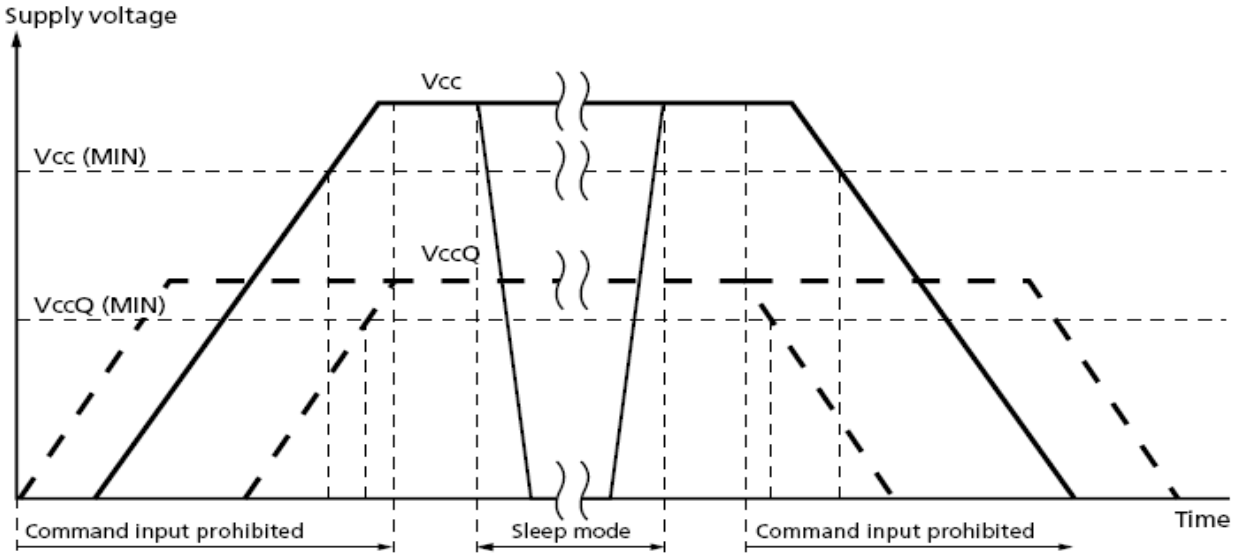
The power-up is handled locally in each device and in the bus master. Below figure shows the power-up sequence. Refer to section 12.3 of the JEDEC Standard Specification No. JESD84-A441 for specific instructions regarding the power-up sequence.



***e*•MMC™ power-up diagram**

4.4. Power cycling

The bus master can execute any sequences of VCC and VCCQ power-up/power down. However, the master must not issue any commands until VCC and VCCQ are stable within each operating voltage range. For more information about power cycling see Section 12.3.3 of the JEDEC Standard Specification No. JESD84-A441 and below figure.



The e•MMC power cycle

4.5. Bus operating conditions

Refer to section 12.5 of the JEDEC Standard Specification No. JESD84-A441.

4.6. Bus signal levels

Refer to section 12.6 of the JEDEC Standard Specification No. JESD84-A441.

4.7. Bus timing

Refer to section 12.7 of the JEDEC Standard Specification No. JESD84-A441.

5. High speed MultiMediaCard operation

All communication between the host and the device is controlled by the host (master). In the following sections, the operation modes and restrictions for controlling the clock signal are defined. For detailed information, refer to section 7 of the JEDEC Standard Specification No. JESD84-A441.

5.1. Boot mode

The host can read boot data from KE44B-26BN/8GB by keeping CMD line Low after power-on or sending CMD0 with argument + 0xFFFFFFFA (optional for slave), before issuing CMD1. The data can be read from either boot area or user area depending on the register setting. Refer to section 7.3 of the JEDEC Standard Specification No. JESD84-A441.

5.2. Write protect management

To allow the host to protect data against erase or write operations, the KE44B-26BN/8GB supports two levels of write protect commands :

- The KE44B-26BN/8GB (including the Boot Area Partitions, General Purpose Area Partition, RPMB, and User/Enhanced User Data Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD.

- Specific segments of the cards may be permanent, power-on or temporarily write protected. ERASE_GROUP_DEF in EXT_CSD decides the segment size. When set to 0, the segment size is defined in units of WP_GRP_SIZE erase groups as specified in the CSD. When set to 1, the segment size is defined in units of HC_WP_GRP_SIZE erase groups as specified in the EXT_CSD.

The SET_WRITE_PROT command sets the write protection of the addressed write protect group, and the CLR_WRITE_PROT command clears the temporary write protection of the addressed write-protect group. The SEND_WRITE_PROT and SEND_WRITE_PROT_TYPE commands are similar to a single block read command. The card shall send a data block containing 32 or 64 write protection bits, respectively, (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units, for densities up to 2GB, and in sector units for densities greater than 2GB. The card will ignore all LSBs below the group size for densities up to 2GB. If the host provides an out of range address as an argument to CMD28, CMD29 or CMD30, the card will reject the command, respond with the ADDRESS_OUT_OF_RANGE bit set and remain in the Tran state.

5.3. Secure erase

In addition to the standard Erase command there is also an optional Secure Erase command. The Secure Erase command differs from the basic Erase command in that it requires the card to execute the erase operation on the memory array when the command is issued and requires the card and host to wait until the operation is complete before moving to the next card operation. Also, the secure erase command requires the card to do a secure purge operation on the erase groups, and any copies of items in those erase groups, identified for erase.

The Secure Erase command is executed in the same way the erase command outlined in Section 7.6.8 of JEDEC Standard Specification No. JESD84-A441, except that the Erase (CMD38) command is executed with argument bit 31 set to 1 and the other argument bits set to zero.
The host should execute the Secure Erase command with caution to avoid unintentional data loss.
Resetting a card (using CMD0, CMD15, or hardware reset for e•MMC™) or power failure will terminate any pending or active Secure Erase command. This may leave the data involved in the operation in an unknown state.

5.4. Secure trim

The Secure Trim command is very similar to the Secure Erase command. The Secure Trim command per-forms a secure purge operation on write blocks instead of erase groups. To minimize the impact on the card's performance and reliability the Secure Trim operation is completed by executing two distinct steps.

- In Secure Trim Step 1 the host defines the range of write blocks that it would like to mark for the secure purge. This step does not perform the actual purge operation. The blocks are marked by defining the start address of the range using the ERASE_GROUP_START (CMD35) command, followed by defining the last address of the range using the ERASE_GROUP_END (CMD36) command. In the case of Secure Trim, both ERASE_GROUP_START and ERASE_GROUP_END arguments are identifying write block addresses. Once the range of blocks has been identified the ERASE (CMD 38) with argument bit 31and 0set to 1 and the remainder of the argument bits set to 0 is applied. This completes Secure Trim Step 1.Secure Trim Step 1 can be repeated several times, with other commands being allowed in between, until all the write blocks that need to be purged have been identified. It is recommended that the Secure Trim Step1 is done on as many blocks as possible to improve its efficiency of the secure trim operation.

- Secure Trim Step 2 issues the ERASE_GROUP_START (CMD35) and ERASE_GROUP_END (CMD36)with addresses that are in range. Note the arguments used with these commands will be ignored. Then the ERASE (CMD 38) with bit 31 and 15 set to 1 and the remainder of the argument bits to 0 is sent. This step actually performs the secure purge on all the write blocks, as well as any copies of those blocks, that were marked during Secure Trim Step 1 and completes the secure trim operation.

Once a write block is marked for erase using Secure Trim Step 1, it is recommended that the host consider this block as erased. However, if the host does write to a block after it has been marked for erase, then the last copy of the block, which occurred as a result of the

modification, will not be marked for erase. All previous copies of the block will remain marked for erase.

5.5. Trim

The Trim operation is similar to the default erase operation described in Section 7.6.8 of JEDEC Standard Specification No. JESD84-A441. The Trim function applies the erase operation to write blocks instead of erase groups. The Trim function allows the host to identify data that is no longer required so that the card can erase the data if necessary during background erase events. The contents of a write block where the trim function has been applied shall be '0' or '1' depending on different memory technology. This value is defined in the EXT_CSD.
Completing the TRIM process is a three steps sequence.

- First the host defines the start address of the range using the ERASE_GROUP_START (CMD35) command
- Next it defines the last address of the range using the ERASE_GROUP_END (CMD36) command.
- Finally it starts the erase process by issuing the ERASE (CMD38) command with argument bit 0 set to one and the remainder of the arguments set to zero.

In the case of a TRIM operation both CMD35 and CMD36 identify the addresses of write blocks rather than erase groups.
If an element of the Trim command (either CMD35, CMD36, CMD38) is received out of the defined erase sequence, the card shall set the ERASE_SEQ_ERROR bit in the status register and reset the whole sequence.
If the host provides an out of range address as an argument to CMD35 or CMD36, the card will reject the command, respond with the ADDRESS_OUT_OF_RANGE bit set and reset the whole erase sequence.
If a “non erase” command (neither of CMD35, CMD36, CMD38 or CMD13) is received, the card shall respond with the ERASE_RESET bit set, reset the erase sequence and execute the last command. Commands not addressed to the selected card do not abort the erase sequence.
If the trim range includes write protected blocks, they shall be left intact and only the non protected blocks shall be erased. The WP_ERASE_SKIP status bit in the status register shall be set.
As described above for block write, the card will indicate that a Trim command is in progress by holdingDAT0 low. The actual erase time may be quite long, and the host may issue CMD7 to deselect the card. The host should execute the Trim command with caution to avoid unintentional data loss. Resetting a card (using CMD0, CMD15, or hardware reset for *e*•MMC™) or power failure will terminate any pending or active Trim command. This may leave the data involved in the operation in an unknown state

5.6. Secure Bad Block management

In some memory array technologies that are used for MulitMediaCards portions of the memory array can become defective with use. In these technologies the card will recover the information from the defective portion of the memory array before it retires the block. This register bit, SEC_BAD_BLK_MGMNT [134] , when set, requires the card to per-form a secure purge on the contents of the defective region before it is retired. This feature requires only those bits that are not defective in the region to be purged.

5.7. Identification mode

While in card identification mode the host resets the card, validates operation voltage range and access mode, identifies the card and assigns a Relative Card Address (RCA) to the card on the bus. All data communication in the Card Identification Mode uses the command line (CMD) only.

5.8. Data transfer mode

The card will enter data transfer mode once an RCA is assigned to it. While the card is in Stand-by State, CMD7 is used to select the card and put it into the Transfer State by including card's relative address in the argument. The host will enter data transfer mode after identifying KE44B-26BN/8GB on the bus.
When the card is in Stand-by State, communication over the CMD and DAT lines will be performed in push-pull mode. Refer to the section 7.6 of the JEDEC Standard Specification No. JESD84-A441 for more detail information.

5.9. Clock control

Refer to section 7.7 of the JEDEC Standard Specification No. JESD84-A441.

5.10. Error conditions

Refer to section 7.8 of the JEDEC Standard Specification No. JESD84-A441.

5.11. Minimum performance

Refer to section 7.9 of the JEDEC Standard Specification No. JESD84-A441.

5.12. Commands

Refer to section 7.10 of the JEDEC Standard Specification No. JESD84-A441.

5.13. Card state transition

Refer to section 7.11 and 7.13 of the JEDEC Standard Specification No. JESD84-A441.

5.14. Response

Refer to section 7.12 of the JEDEC Standard Specification No. JESD84-A441.

5.15. Timing diagrams and values

Refer to section 7.15 of the JEDEC Standard Specification No. JESD84-A441.

5.16. Background Operations

Devices have various maintenance operations need to perform internally. In order to reduce latencies during time critical operations like read and write, it is better to execute maintenance operations in other times - when the host is not being serviced. Operations are then separated into two types: •Foreground operations – operations that the host needs serviced such as read or write commands; •Background operations – operations that the device executes while not servicing the host; In order for the device to know when the host does not need it and it can execute background operations, host shall write any value to BKOPS_START (EXT_CSD byte [164]) to manually start background operations. Device will stay busy till no more background processing is needed.Refer to the section 7.6.19 of the JEDEC Standard Specification No. JESD84-A441 for more detail information.

5.17. High Priority Interrupt (HPI)

In some scenarios, different types of data on the device may have different priorities for the host. For example, writing operation may be time consuming and therefore there might be a need to suppress the writing to allow demand paging requests in order to launch a process when requested by the user. The high priority interrupt (HPI) mechanism enables servicing high priority requests, by allowing the device to interrupt a lower priority operation before it is actually completed, within OUT_OF_INTERRUPT_BUSY_TIME timeout. Host may need to repeat the interrupted operation or part of it to complete the original request. The HPI command may have one of two implementations in the device:•CMD12 – based on STOP_TRANSMISSION command when the HPI bit in its argument is set.•CMD13 – based on SEND_STATUS command when the HPI bit in its argument is set. Host shall check the read-only HPI_IMPLEMENTATION bit in HPI_FEATURES (EXT_CSD byte [503])and use the appropriate command index accordingly.

Interruptible commands

CMD Index	Name	Is interruptible?	Restrictions
CMD24	WRITE_BLOCK	Yes	
CMD25	WRITE_MULTIPLE_BLOCK	Yes	
CMD38	ERASE	Yes	
CMD6	SWITCH	Yes	Only interruptible when writing to the BKOPS_START field in EXT_CSD
All others		No	

Refer to the section 7.6.20 of the JEDEC Standard Specification No. JESD84-A441 for more detail information.

6. Card registers

There are six different registers are defined within the card interface :

- Operation conditions register (OCR)
- Card identification register (CID)
- Card specific data register (CSD)
- Relative card address register (RCA)
- DSR (driver stage register)
- Extended card specific data register (EXT_CSD).

6.1. Operation conditions register (OCR)

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the card and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. For further details, refer to section 8.1 of the JEDEC Standard Specification No. JESD84-A441.

OCR register definitions

OCR bit	VDD voltage window	High Voltage MultiMediaCard	Dual voltage MultiMediaCard and e-MMC™
[6:0]	Reserved	00 00000b	00 00000b
[7]	1.70 - 1.95V	0b	1b
[14:8]	2.0-2.6V	000 0000b	000 0000b
[23:15]	2.7-3.6V	1 1111 1111b	1 1111 1111b
[28:24]	Reserved	0 0000b	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)	00b (byte mode) 10b (sector mode)
[31]	(card power up status bit (busy)[1]		

1) This bit is set to LOW if the card has not finished the power up routine

6.2. Card identification (CID) register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase (MultiMediaCard protocol). Every individual flash or I/O card shall have an unique identification number. For details, refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A441

CID fields

Parameter	Description	Width	CID slice	Value
MID	Manufacturer ID	**8**	[127:120]	**70h**
	Reserved	**6**	[119:114]	**00h**
CBX	Card BGA	**2**	[113:112]	**01h**
OID	OEM/Application ID	**8**	[111:104]	**00h**
PNM	Product name	**48**	[103:56]	**4D4D43303847h("MMC8G")**
PRV	Product revision	**8**	[55:48]	**44h**
PSN	Product serial number	**32**	[47:16]	**Random by Production**
MDT	Manufacturing date	**8**	[15:8]	**month, year**
CRC	CRC7 checksum	**7**	[7:1]	**30h**
-	Not used,always'1"	**1**	[0]	**1h**

6.3. Card specific data register (CSD)

The Card-Specific Data (CSD) register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed,whether the DSR register can be used etc. For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A441.

CSD fields

Parameter	Description	Width	CSD Slice	Value
CSD_STRUCTURE	CSD structure	**2**	[127:126]	**3h**
SPEC_VERS	System specification version	**4**	[125:122]	**4h**
-	Reserved	**2**	[121:120]	**0h**
TAAC	Data read access-time 1	**8**	[119:112]	**4Fh**
NSAC	Data read access-time 2 in CLK cycles (NSAC*100)	**8**	[111:104]	**1h**
TRAN_SPEED	Max. bus clock frequency	**8**	[103:96]	**32h**
CCC	Card command classes	**12**	[95:84]	**F5h**
READ_BL_LEN	Max. read data block length	**4**	[83:80]	**9h**
READ_BL_PARTIAL	Partial blocks for read allowed	**1**	[79:79]	**0h**
WRITE_BLK_MISALIGN	Write block misalignment	**1**	[78:78]	**0h**

READ_BLK_MISALIGN	Read block misalignment	**1**	[77:77]	**0h**
DSR_IMP	DSR implemented	**1**	[76:76]	**0h**
-	Reserved	**2**	[75:74]	**0h**
*C_SIZE	Device size	**12**	[73:62]	**FFFh**
VDD_R_CURR_MIN	Max. read current @ VDD min	**3**	[61:59]	**7h**
VDD_R_CURR_MAX	Max. read current @ VDD max	**3**	[58:56]	**7h**
VDD_W_CURR_MIN	Max. write current @ VDD min	**3**	[55:53]	**7h**
VDD_W_CURR_MAX	Max. write current @ VDD max	**3**	[52:50]	**7h**
C_SIZE_MULT	Device size multiplier	**3**	[49:47]	**7h**
ERASE_GRP_SIZE	Erase group size	**5**	[46:42]	**1Fh**
ERASE_GRP_MULT	Erase group size multiplier	**5**	[41:37]	**1Fh**
WP_GRP_SIZE	Write protect group size	**5**	[36:32]	**Fh**
WP_GRP_ENABLE	Write protect group enable	**1**	[31:31]	**1h**
DEFAULT_ECC	Manufacturer default	**2**	[30:29]	**0h**
R2W_FACTOR	Write speed factor	**3**	[28:26]	**2h**
WRITE_BL_LEN	Max. write data block length	**4**	[25:22]	**9h**
WRITE_BL_PARTIAL	Partial blocks for write allowed	**1**	[21:21]	**0h**
-	Reserved	**4**	[20:17]	**0h**
CONTENT_PROT_APP	Content protection application	**1**	[16:16]	**0h**
FILE_FORMAT_GRP	File format group	**1**	[15:15]	**0h**
COPY	Copy flag (OTP)	**1**	[14:14]	**0h**
PERM_WRITE_PROTECT	Permanent write protection	**1**	[13:13]	**0h**
TMP_WRITE_PROTECT	Temporary write protection	**1**	[12:12]	**0h**
FILE_FORMAT	File format	**2**	[11:10]	**0h**
ECC	ECC code	**2**	[9:8]	**0h**
CRC	Calculated CRC	**7**	[7:1]	**30h**
-	Not used, always ‘1’	**1**	[0]	**1h**

6.4. Extended CSD register

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A441.

Extended CSD

Parameter	Description	ECSD slice	Value
-	Reserved	[511:505]	**0h**
S_CMD_SET	Supported Command Sets	[504]	**1h**
HPI_FEATURES	HPI Features	[503]	**3h**
BKOPS_SUPPORT	Background operations support	[502]	**1h**
-	Reserved	[501:247]	**0h**
BKOPS_STATUS	Background operations status	[246]	**0h**
CORRECTLY_PRG_SECTORS_NUM	Number of correctly programmed sectors	[245:242]	**0h**
INI_TIMEOUT_AP	1st Initialization time after partitioning	[241]	**E6h**
-	Reserved	[240]	**0h**
PWR_CL_DDR_52_360	Power class for 52MHz, DDR @ 3.6V	[239]	**0h**
PWR_CL_DDR_52_195	Power class for 52MHz, DDR @ 1.95V	[238]	**0h**
-	Reserved	[237:236]	**0h**
MIN_PERF_DDR_W_8_52	Minimum Write Performance for 8bit @ 52MHz in DDR Mode	[235]	**0h**
MIN_PERF_DDR_R_8_52	Minimum Read Performance for 8bit @ 52MHz in DDR Mode	[234]	**0h**
-	Reserved	[233]	**0h**
TRIM _MULT	TRIM Multiplier	[232]	**0h**
SEC_FEATURE_SUPPORT	Secure Feature support	[231]	**15h**
SEC_ERASE_MULT	Secure Erase Multiplier	[230]	**0h**
SEC_TRIM_MULT	Secure TRIM Multiplier	[229]	**0h**
BOOT_INFO	Boot Information	[228]	**7h**
-	Reserved	[227]	**0h**
BOOT_SIZE_MULTI	Boot partition size	[226]	**10h**
ACCESS_SIZE	Access size	[225]	**7h**
HC_ERASE_GROUP_SIZE	High Capacity Erase unit size	[224]	**8h**
ERASE_TIMEOUT_MULT	High capacity erase time out	[223]	**0h**
REL_WR_SEC_C	Reliable write sector count	[222]	**8h**
HC_WP_GRP_SIZE	High capacity write protect group size	[221]	**2h**
S_C_VCC	Sleep current [VCC]	[220]	**8h**
S_C_VCCQ	Sleep current [VCCQ]	[219]	**8h**
-	Reserved	[218]	**0h**
S_A_TIMEOUT	Sleep/Awake time out	[217]	**10h**
-	Reserved	[216]	**0h**
SEC_COUNT	Sector count	[215:212]	**E66000h**
-	Reserved	[211]	**0h**
MIN_PERF_W_8_52	Minimum Write Performance for 8bit @52MHz	[210]	**8h**

MIN_PERF_R_8_52	Minimum Read Performance for 8bit @52MHz	[209]	**8h**
MIN_PERF_W_8_26_4_52	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	[208]	**8h**
MIN_PERF_R_8_26_4_52	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	[207]	**8h**
MIN_PERF_W_4_26	Minimum Write Performance for 4bit @26MHz	[206]	**8h**
MIN_PERF_R_4_26	Minimum Read Performance for 4bit @26MHz	[205]	**8h**
-	Reserved	[204]	**0h**
PWR_CL_26_360	Power Class for 26MHz @ 3.6V	[203]	**0h**
PWR_CL_52_360	Power Class for 52MHz @ 3.6V	[202]	**0h**
PWR_CL_26_195	Power Class for 26MHz @ 1.95V	[201]	**0h**
PWR_CL_52_195	Power Class for 52MHz @ 1.95V	[200]	**0h**
PARTITION_SWITCH_TIME	Partition switching timing	[199]	**1h**
OUT_OF_INTERRUPT_TIME	Out-of-interrupt busy timing	[198]	**2h**
-	Reserved	[197]	**0h**
CARD_TYPE	Card Type	[196]	**Fh**
-	Reserved	[195]	**0h**
CSD_STRUCTURE	CSD Structure Version	[194]	**2h**
	Reserved	[193]	**0h**
EXT_CSD_REV	Extended CSD Revision	[192]	**5h**
CMD_SET	Command Set	[191]	**0h**
-	Reserved	[190]	**0h**
CMD_SET_REV	Command Set Revision	[189]	**0h**
	Reserved	[188]	**0h**
POWER_CLASS	Power Class	[187]	**0h**
-	Reserved	[186]	**0h**
HS_TIMING	High Speed Interface Timing	[185]	**1h**
-	Reserved	[184]	**0h**
BUS_WIDTH	Bus Width Mode	[183]	**2h**
-	Reserved	[182]	**0h**
ERASE_MEM_CONT	Content of explicit erased memory range	[181]	**0h**
-	Reserved	[180]	**0h**
PARTITION_CONFIG	Partition Configuration	[179]	**0h**
BOOT_CONFIG_PROT	Boot config protection	[178]	**0h**
BOOT_BUS_WIDTH	Boot bus width1	[177]	**0h**
	Reserved	[176]	**0h**
ERASE_GROUP_DEF	High-density erase group definition	[175]	**0h**
-	Reserved	[174]	**0h**
BOOT_WP	Boot area write protect register	[173]	**0h**
-	Reserved	[172]	**0h**
USER_WP	User area write protect register	[171]	**0h**

-	Reserved	[170]	**0h**
FW_CONFIG	FW Configuration	[169]	**0h**
RPMB_SIZE_MULT	RPMB Size	[168]	**1h**
WR_REL_SET	Write reliability setting register	[167]	**0h**
WR_REL_PARAM	Write reliability parameter register	[166]	**0h**
-	Reserved	[165]	**0h**
BKOPS_START	Manually start background operations	[164]	**0h**
BKOPS_EN	Enable background operations handshake	[163]	**0h**
RST_n_FUNCTION	H/W reset function	[162]	**0h**
HPI_MGMT	HPI management	[161]	**0h**
PARTITIONING SUPPORT	Partitioning support	[160]	**3h**
MAX_ENH_SIZE_MULT	Max Enhanced Area Size	[159:157]	**1B2h**
PARTITIONS_ATTRIBUTE	Partitions Attribute	[156]	**0h**
GP_SIZE_MULT	General Purpose Partition Size	[154:143]	**0h**
ENH_SIZE_MULT	Enhanced User Data Area Size	[142:140]	**0h**
ENH_START_ADDR	Enhanced User Data Start Address	[139:136]	**0h**
-	Reserved	[135]	**0h**
SEC_BAD_BLK_MGMNT	Bad Block Management mode	[134]	**0h**
-	Reserved	[133:0]	**0h**

6.5. RCA (relative card address) register

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7. For details refer to section 8.5 of the JEDEC Standard Specification No. JESD84-A441.

6.6. DSR (driver stage register) register

The 16-bit driver stage register (DSR) is described in detail in Section 8.6 of the JEDEC Standard Specification No. JESD84-A441. It can be option-ally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

7. Appendix

7.1. Electrical Specifications of MMC controller

Absolute Maximum Rating

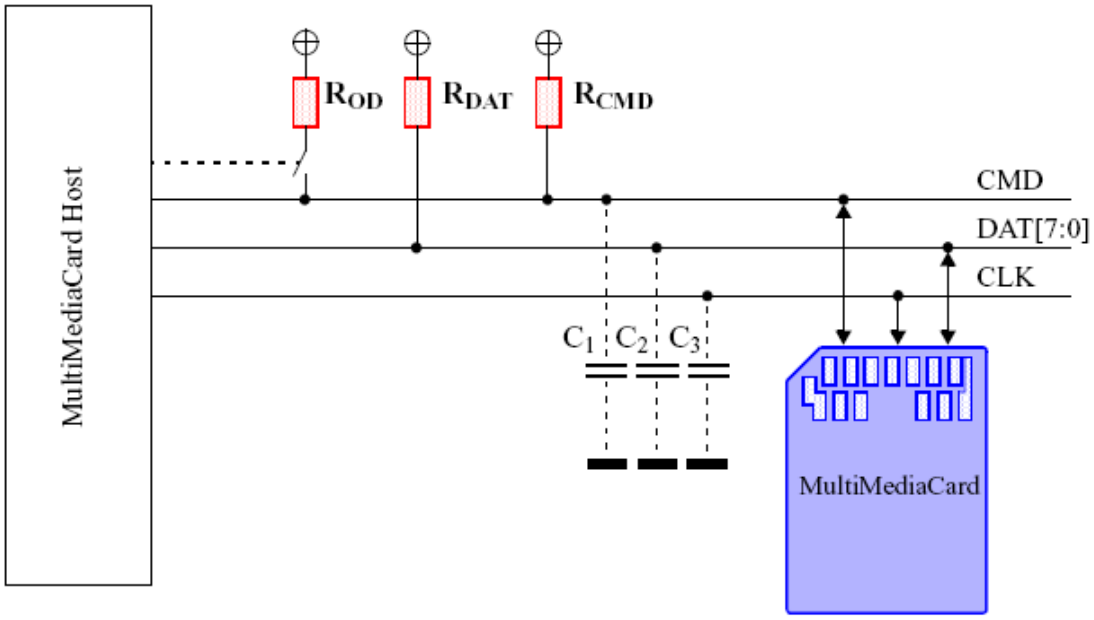
Parameter	Symbol	Min	MAX	Unit
Operating Temperature	T_a	- 25	+85	℃
V_{DD} Voltage	V_{DD}	2.7	3.6	V

7.2. The MultiMediaCard (MMC) bus

The MultiMediaCard bus has ten communication lines and three supply lines:

- CMD : Command is a bidirectional signal. The host and card drivers are operating in two modes, open drain and push/pull.
- DAT0-7 : Data lines are bidirectional signals. Host and card drivers are operating in push-pull mode
- CLK : Clock is a host to card signal. CLK operates in push-pull mode
- VDD : VDD is the power supply line for all cards.
- VSS1, VSS2 are two ground lines.

(a)Bus circuitry diagram



(b)Capacitance :

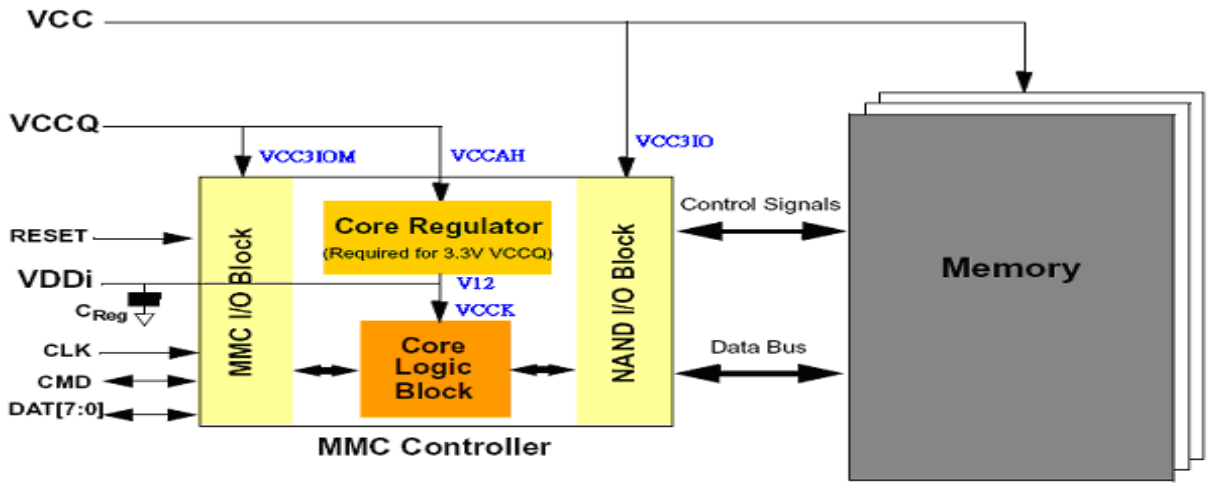
Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100(1)	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10		100(1)	Kohm	to prevent bus floating
Internal pull up resistance DAT1–DAT7	R_{int}	10		150	kohm	to prevent unconnected lines floating
Bus signal line capacitance	C_L			30	pF	Single card
Single card capacitance	C_{MICRO}			12	pF	For MMC*micro*
	C_{MOBILE}			18		For MMC*mobile* and MMC*plus*
	C_{BGA}		7	12		For BGA
Maximum signal line inductance				16	nH	$f_{PP} \leq 52$ MHz

(1) Recommended maximum pull-up is 50Khom for 1.8V interface supply voltages. A 3V part may use the whole range up to 100Kohms.

7.3. *e*•MMC™ Power supply

In the e•MMC™, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage. The core regulator is optional and only required when VCCQ is in the 3V range. A Creg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

7.3.1. e•MMC™ internal power diagram



Recommended Power Domain Connections:

(a) VCCQ : Capacitors : 0.1uF , 1uF
(b) VCC : Capacitors : 0.1uF , 1uF
(c) **VDDi : Capacitors : 0.1uF , 1uF**

7.3.2. *e*•MMC™ power supply voltage

The e•MMC™ supports one or more combinations of VCC and VCCQ as shown in below table. The VCCQ must be defined at equal to or less than VCC.

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 1.8V	tPRUL		25	ms	

7.3.3. *e*•MMC™ voltage combinations

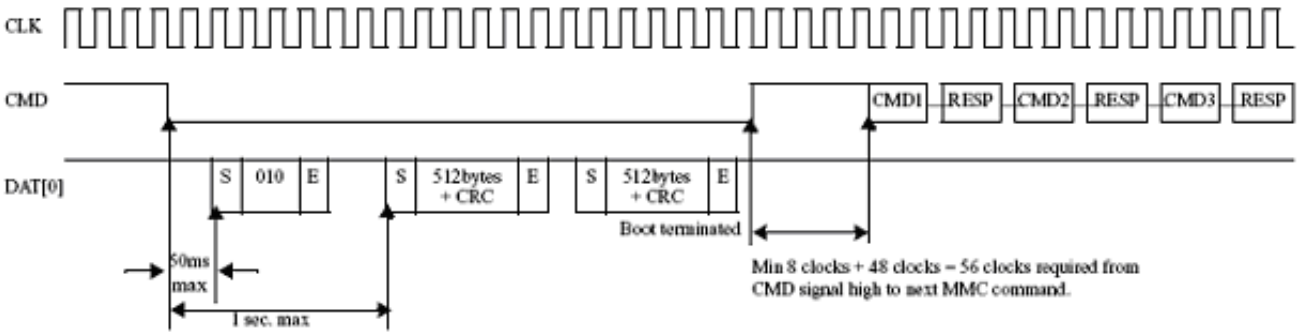
The e•MMC™ must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations.

		VccQ	
		1.65V–1.95V	**2.7V–3.6V**
Vcc	**2.7V-3.6V**	Valid	Valid

7.4. Boot operation mode

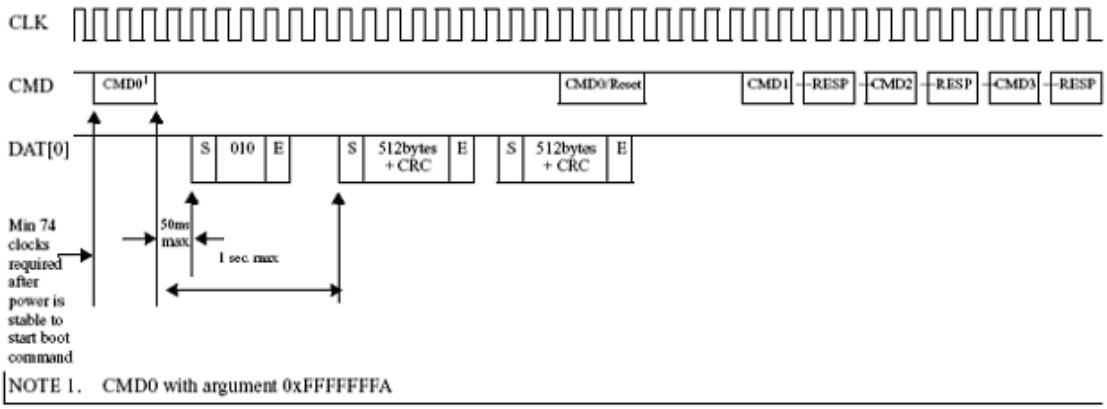
In boot operation mode, the master (MultiMediaCard host) can read boot data from the slave (MMC device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.

MultiMediaCard state diagram (boot mode) – CMD line low



MultiMediaCard state diagram (boot mode)

MultiMediaCard state diagram (alternative boot mode) - CMD0 with argument + 0xFFFFFFFA



MultiMediaCard state diagram (alternative boot mode)

7.5. DC Characters

7.5.1. Bus operating conditions

Parameter		Symbol	Min	Max	Unit	Remark
Peak voltage on all lines	Card		-0.5	VDD + 0.5	V	
	BGA		-0.5	VCCQ + 0.5	V	
All Inputs						
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)			-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	µA	
All Outputs						
Output Leakage Current (before initialization sequence)			-100	100	µA	
Output Leakage Current (after initialization sequence)			-2	2	µA	

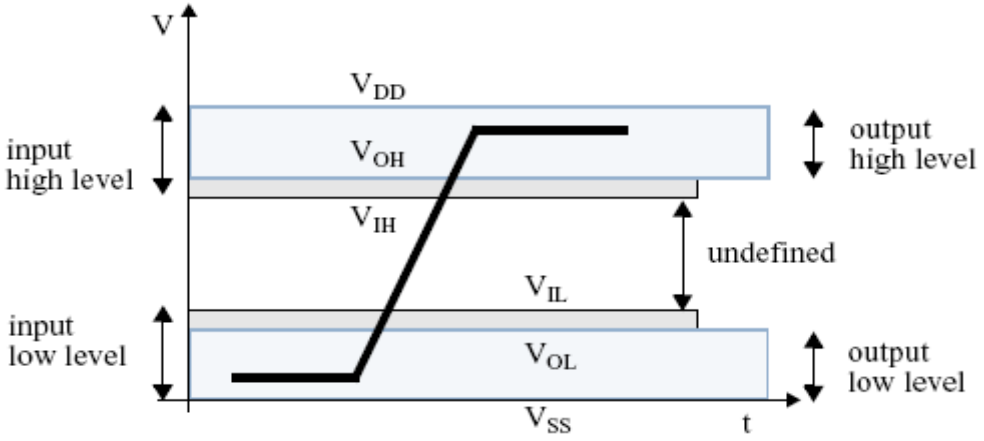
7.5.2. Power Supply - High Voltage MultiMediaCard

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	VDD	2.7	3.6	V	
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Supply power-up	tPRU	-	35	ms	

7.5.3. Power Supply Voltage - Dual voltage MultiMediCard

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage (low voltage range)	VDDL	1.70	1.95	V	1.95V ~ 2.7V range is not supported
Supply voltage (high voltage range)	VDDH	2.7	3.6	V	
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Supply power-up (low voltage range)	tPRUL	-	25	ms	
Supply power-up (high voltage range)	tPRUH	-	35	ms	

7.6. Bus Signal Levels



7.6.1. Open-Drain Mode Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD-0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

7.6.2. Push-Pull Mode Bus Signal Level - High Voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75*VDD		V	IOH=-100 µA @VDD min
Output LOW voltage	VOL		0.125*VDD	V	IOL=100 µA @VDD min
Input HIGH voltage	VIH	0.625*VDD	VDD + 0.3	V	
Input LOW voltage	VIL	VSS-0.3	0.25*VDD	V	

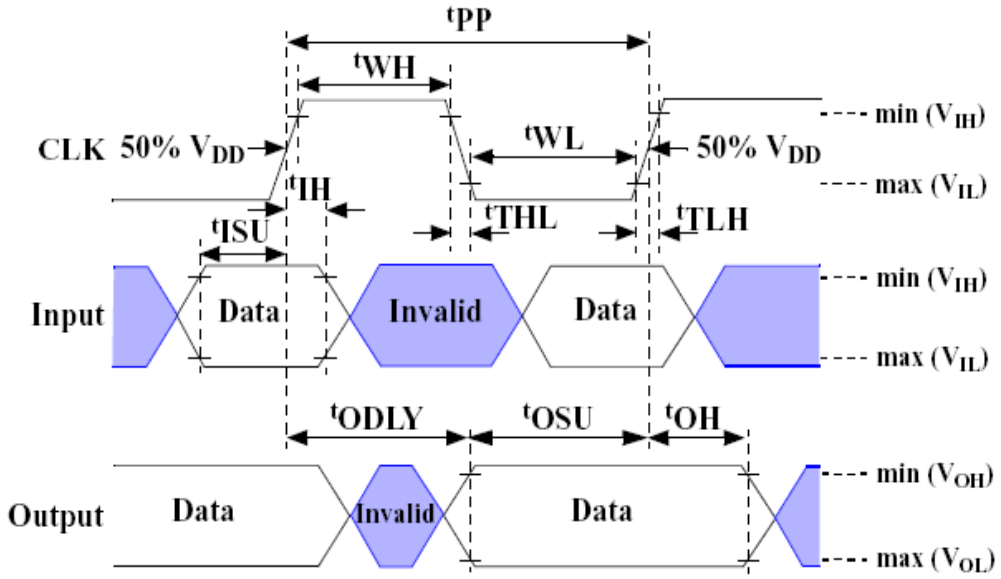
7.6.3. Push-Pull Mode Bus Signal Level - Dual voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	VDD- 0.45V		V	IOH=-2mA
Output LOW voltage	VOL		0.45V	V	IOL=2mA
Input HIGH voltage	VIH	0.65 * VDD (1)	VDD + 0.3	V	
Input LOW voltage	VIL	VSS-0.3	0.35 * VDD (2)	V	

(1)0.7 * VDD for MMC 4.3 and older revisions.
(2)0.3 * VDD for MMC 4.3 and older revisions.

7.7. AC characters

7.7.1 Bus timing



Data must always be sampled on the rising edge of the clock.

7.7.2. High Speed Card Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	$C_L \le 30$ pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t_{WH}	6.5		ns	$C_L \le 30$ pF
Clock low time	t_{WL}	6.5		ns	$C_L \le 30$ pF
Clock rise time[4]	t_{TLH}		3	ns	$C_L \le 30$ pF
Clock fall time	t_{THL}		3	ns	$C_L \le 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \le 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \le 30$ pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	$C_L \le 30$ pF
Output hold time	t_{OH}	2.5		ns	$C_L \le 30$ pF
Signal rise time[5]	t_{RISE}		3	ns	$C_L \le 30$ pF
Signal fall time	t_{FALL}		3	ns	$C_L \le 30$ pF

NOTE 1. CLK timing is measured at 50% of V_{DD}.
NOTE 2. A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
NOTE 3. Card can operate as high-speed card interface timing at 26 MHz clock frequency.
NOTE 4. CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).
NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

7.7.3 High Speed Card Interface Timing Backwards Compatible Card Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Clock CLK[2]					
Clock frequency Data Transfer Mode (PP)[3]	f_{PP}	0	26	MHz	$C_L \leq 30$ pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock high time	t_{WH}	10			$C_L \leq 30$ pF
Clock low time	t_{WL}	10		ns	$C_L \leq 30$ pF
Clock rise time[4]	t_{TLH}		10	ns	$C_L \leq 30$ pF
Clock fall time	t_{THL}		10	ns	$C_L \leq 30$ pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	$C_L \leq 30$ pF
Input hold time	t_{IH}	3		ns	$C_L \leq 30$ pF

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	t_{OSU}	11.7		ns	$C_L \leq 30$ pF
Output hold time[5]	t_{OH}	8.3		ns	$C_L \leq 30$ pF

NOTE 1. The card must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

NOTE 2. CLK timing is measured at 50% of VDD.

NOTE 3. For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.

NOTE 4. CLK rise and fall times are measured by min (V_{IH}) and max (V_{IL}).

NOTE 5. tOSU and tOH are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.
Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the systemor to use slow clock frequency, so that host could have data set up margin for those devices.
In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

7.7.4. Dual data rate interface timings

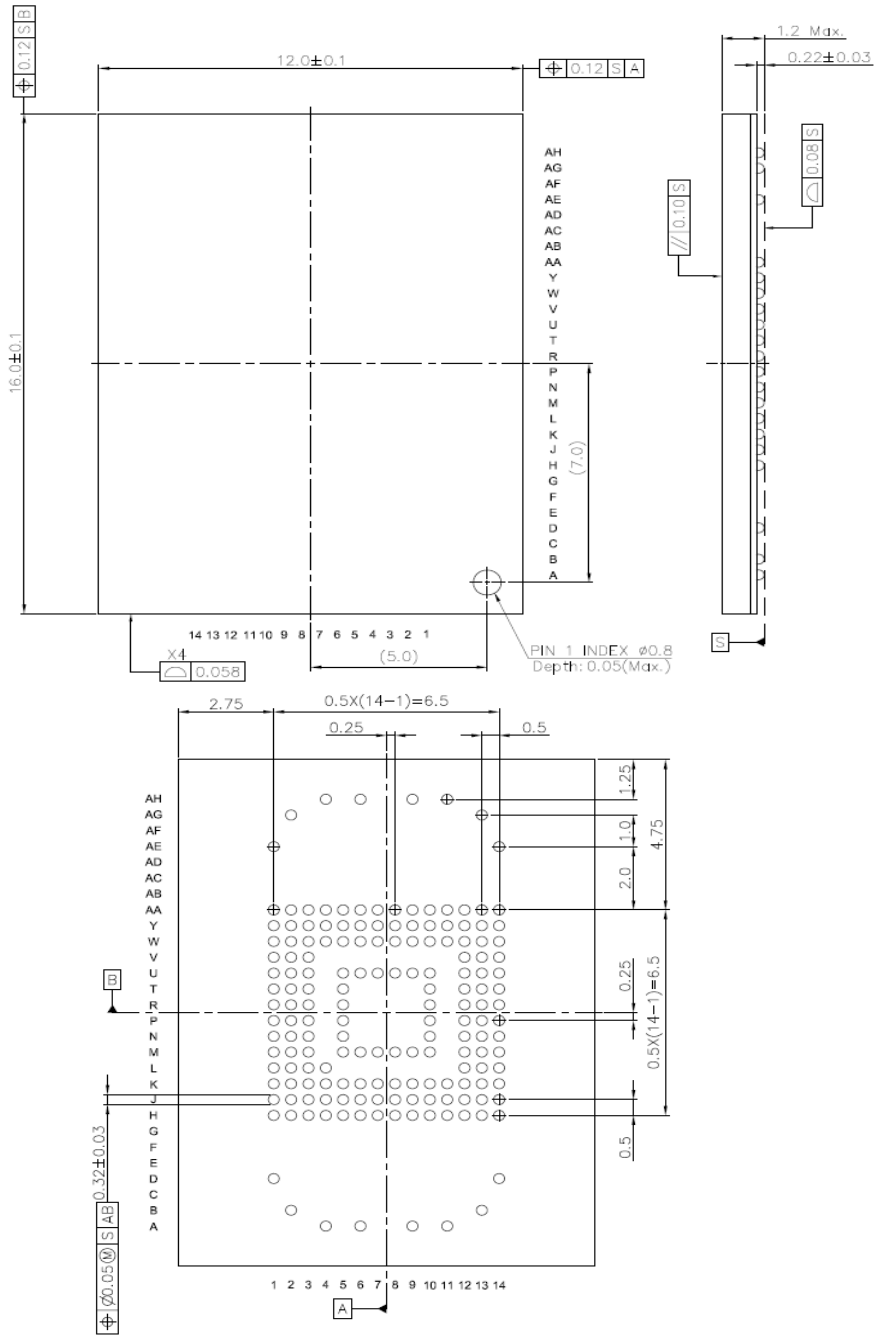
Parameter	Symbol	Min	Max.	Unit	Remark[1]
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

NOTE 1. CLK timing is measured at 50% of VDD.
NOTE 2. Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL)

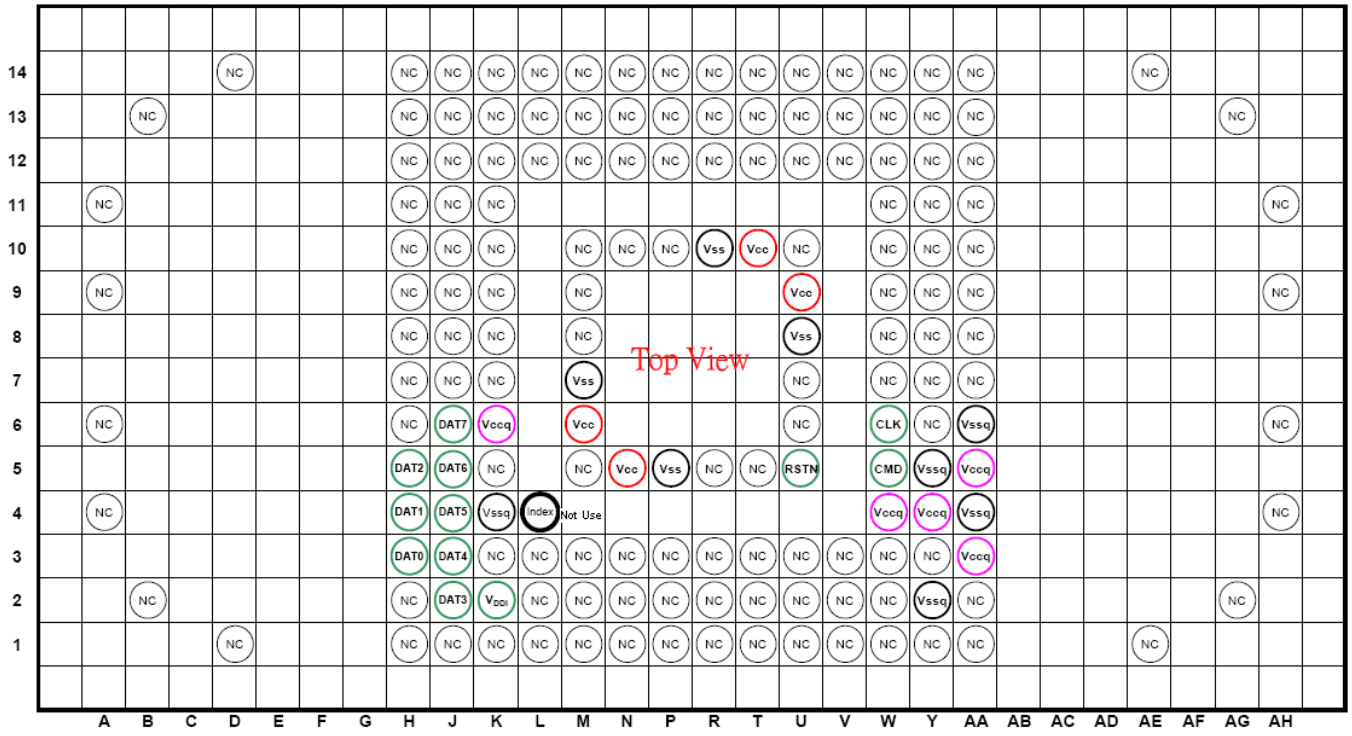
8. Package connections

8.1. Package Mechanical

a)169 ball FBGA(12.0 X 16.0 X 1.2mm)



Top view through package


Top View
Index
Not Use
DAT2
DAT6
DAT1
DAT5
DAT0
DAT4
DAT7
DAT3
Vccq
Vssq
Vcc
Vss
CLK
CMD
RSTN
NC
A B C D E F G H J K L M N P R T U V W Y AA AB AC AD AE AF AG AH
14 13 12 11 10 9 8 7 6 5 4 3 2 1

Revision History

Rev.	History	Date	Remark
0.1	Preliminary	May/1/2010	
0.2	Update *e*·MMC™ trademark	June/1/2010	
0.3	1. Update System Performance 2. Add Recommended Power Domain Connections in section 7.3.1	July/1/2010	
0.4	1. Version *e*·MMC™ 4.41 included 2. KE44B-26BN/16GB included	Oct/1/2010	
0.5	Delete KE44B-25AN/2GB & KE44B-26BN/16GB	Feb/2011	
0.6	Add the weight of product	Mar/2011	
0.7	1. Separate the 4GB and the 8GB of spec. 2. Add the values of register	May/2011	
1.0	Released 1.0 Ver.	Jun/2011	
1.1	1. Revise the value of register. 2. Revise the description (see Section 5 on page 11). 3. Revise the description (see Section 5.2 on page 12). 4. Revise 7.6.9 to 7.6.8 of JEDEC (see Section 5.3 on page 12). 5. Revise 7.6.11 to 7.6.8 of JEDEC (see Section 5.5 on page 14). 6. Revise "This bit is set to LOW if the card has …." (see Section 6.1 on page 17).	Sep/2011	