DALLAS SEMICONDUCTOR

Tech Brief 1
MicroLAN Design Guide

What is the 1-Wire net?

The 1-Wire® net, sometimes known as a MicroLAN, is a low cost bus based on a PC or microcontroller communicating digitally over twisted pair cable with 1-Wire® components. The network is defined with an open drain (wired-AND) master/slave multidrop architecture that uses a resistor pull-up to a nominal 5V supply at the master. A 1-Wire net based system consists of three main elements: a bus master with controlling software, the wiring and associated connectors and 1-Wire devices. The 1-Wire net allows tight control because no node is allowed to speak unless requested by the master, and no communication is allowed between slaves, except through the master.

Any standard microcontroller such as an 8051 with a 1.8MHz or greater clock, as well as a PC using a 115.2 kbps capable UART can serve as master for the net. The UART supplies 1-Wire timing by sending a byte for each 1-Wire bit, creating short and long time slots to encode the binary 1's and 0's. At this 14.4 kbps data rate (115.2 divided by 8 =14.4 kbps) the PC can address a node on the bus and start receiving data in less than 7 milliseconds. Since timing is controlled by the UART, microprocessor clock speed does not affect the time required to find and read a slave ID on the net. **Diagram 1** illustrates a portion of a typical communication sequence for 1-Wire protocol. Software such as TMEX™ to control and monitor bus activity is available for downloading at www.ibutton.com/software/tmex/index/html.

1-Wire net protocol uses conventional CMOS/TTL logic levels, where 0.8V or less indicates a logic zero and 2.2V or greater represents a logic one. Operation is specified over a supply voltage range of 2.8 to 6 volts. Both the master and slaves are configured as transceivers allowing data to flow in either direction, but only one direction at a time. Technically speaking, data transfers are half-duplex and bit sequential over a single pair of wires, data and return, from which the slaves "steal" power by use of an internal diode and capacitor. Data is read and written least significant bit first. An economical, DS9097 COM Port Adapter is available to interface RS232 to the net. Newer more versatile adapters based on the DS2480 Serial 1-Wire Line Driver chip provide more capability such as active pull-up and slew-rate control. The DS2480 is designed to interface between RS232 and the 1-Wire bus generating the proper signals and programmable waveforms that provide maximum performance. Regardless of whether a DS9097 or a DS2480 based adapter is used, readily available, low capacitance, unshielded, Category 5 twisted pair phone wire is recommended for the bus.

As previously mentioned, data on the 1-Wire net is transferred with respect to time slots. For example, to write a logic one to a 1-Wire device, the master pulls the bus low and holds it for 15 microseconds or less. To write a logic zero, the master pulls the bus low and holds it for at least 60 microseconds to pro-

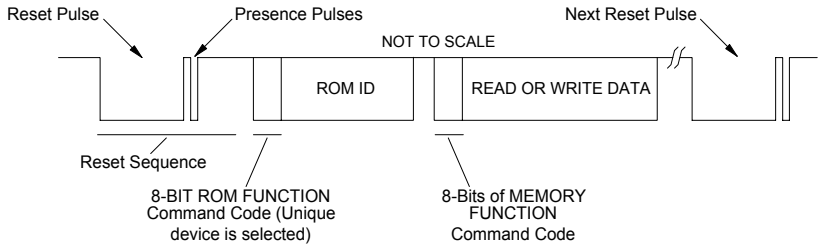

Diagram 1 A typical 1-Wire communication sequence.

vide timing margin for worse case conditions. A system clock is not required, as each 1-Wire part is self clocked by its own internal oscillator that is synchronized to the falling edge of the master. Power for chip operation is derived from the bus during idle communication periods when the DATA line is at 5V by including a half wave rectifier onboard each slave.

In **Figure 1**, whenever the data line is pulled high by the bus pull-up resistor the diode in the half wave rectifier turns on and charges the internal 800pF capacitor. When it drops below the voltage on the capacitor, the diode is reverse biased, isolating the charge. The isolated charge stored on the capacitor provides the energy source to power the slave during the intervals the bus is pulled low. The amount of charge lost during these periods is proportional to the time the bus is low. It is replenished when the data line again turns on the half wave rectifier diode. This concept of "stealing" power from the data line by a half wave rectifier is referred to as "parasite power."

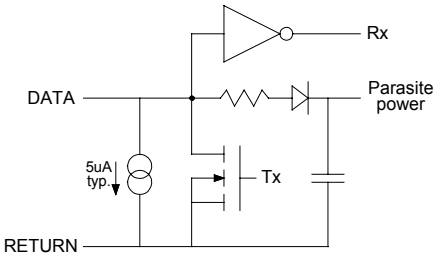

Figure 1 1-Wire parasite power circuit.

In operation, the master resets the network by holding the bus low for at least 480 microseconds, (**Diagram 1** again) releasing it, and then looking for a responding Presence pulse from a slave connected to the line. If a Presence pulse is detected, it then accesses the slave by calling its address. The master issues any device specific commands required, and performs any needed data transfers between it and the slave. It controls the information transfer by generating time slots and examining the response from the slave. For a more detailed description of the communication sequence, refer to "So that's how it works!" in Chapter 2. Complete technical and timing details are available in the Book of DS19xx iButton® Standards.

Within each 1-Wire slave created is stored a lasered ROM section with its own guaranteed unique, 64-bit serial number that acts as its node address. This unique address is composed of eight bytes divided into three main sections. Starting with the LSB, the first byte stores the 8-bit family code that identifies the device type. The next 6 bytes store a customizable 48-bit individual address while the last byte (MSB) contains a cyclic redundancy checksum (CRC) with a value based on the data contained in the first seven bytes. This allows the master to determine if an address was read without error. With 2^{48} serial numbers available, conflicting or duplicate node addresses on the LAN will never be a problem.

Floppy in a Button

1-Wire devices can be formatted with a file directory just like a floppy disk. This allows files to be randomly accessed and changed without disturbing other records. Information is read or written when a device connected to the bus is addressed by the master, or an identification badge or Decoder Ring is touched to a port somewhere along the 1-Wire net. A typical access port consists of outer ring and insulated spring loaded center conductors mounted in an appropriate housing. The ring touches the case of the iButton or Decoder Ring and connects it to the return line of the bus while the spring loaded center contact connects the lid to the bus data line.

The inclusion of up to 64K of memory in 1-Wire chips allows standard information such as employee name, ID number etc., to be stored within the device. For example, it would only take about one fourth of the available memory to store the equivalent of a business card and digitized black and white photo ID. This still leaves space for additional important data such as medical records, credit information or security level to be included. With such information literally "at hand" in the case of the Decoder Ring, reliable identification and access is readily available and machine readable. Memory devices are also useful for storing "tag" information for nodes on the bus and for sensor calibration or function information.

Packaged and ready to go

Because the 1-Wire net only requires a single wire plus return, iButtons can be packaged in a coin style battery case 16mm in diameter, and 5.8mm thick. This is about the size of a stack of five dimes. The two piece stainless steel package acts as both protective housing and electrical connection point. The case serves as return contact (ground), and the lid as data contact. The package size allows inclusion of a Lithium cell to provide 10 years of standby power to maintain data in volatile RAM memory when not connected to the net. A variety of memory configurations are available, including iButtons containing up to 64K of memory. 1-Wire devices that do not require a memory backup battery are also available in more traditional solder-mount packages.

SECTION 2
Working the LAN

Control the slew rate of the driver

In a typical system using a PC running Dallas' 1-Wire Operating System Software (TMEX) and using a COM port adapter, communication occurs in time slots of 8.68 microseconds under control of the UART. A communication cycle begins when the transistor in the master actively pulls the line to a logic zero. This one to zero transition is the synchronizing edge for all 1-Wire communications. A 1-wire slave holds the zero if appropriate, and the resistor returns the line to the supply voltage after both the master and slave release the line. In ROM search, which is required to identify the devices on the bus, the most critical part of 1-Wire communication is the read data time slot, especially if a one is being transmitted. In the general case, there may be many arbitrarily placed devices on the bus, each seeing the falling edge of the time slot issued by the master at a slightly different time. Because communication requires that a signal travel the length of the cable and return, the electrical length of the bus must be less than one half the time interval allowed for a single data bit slot. That is, round trip propagation time for a signal must be less than 4.34 microseconds (8.68 microseconds divided by 2). Devices beyond this range will not be seen by the master.

In the COM port adapter, there is an active pull down transistor that is either turned fully on or completely off under control of the bus master. The falling edge generated by turning it on signals the start of a time slot on the net. When the switch is turned off, the line is pulled toward the supply voltage by the bus pull-up resistor. Due to the rapid response and low impedance of the active pull down transistor used to generate a logic zero, the signal fall time will be in the sub-microsecond range. If switching occurs in less time than the transition takes to traverse the electrical length of the cable and return, the 1-Wire net is operating in a transmission line environment and reflections from the line end can disrupt communications.

Normally, the solution would be to terminate the ends of the cable in its characteristic impedance with fixed resistors. These resistors would then absorb the energy that otherwise would be reflected by the impedance mismatch and cause communications problems. Unfortunately, the recommended cabling has a 100 Ohm typical impedance which would result in the inability to generate a logic one with an acceptable pull-up resistor value. It is interesting to note that since the port transistor inside 1-Wire devices has a 100 Ohm on-resistance, the bus is properly terminated anytime one at the cable end is turned on. It may be possible on some 1-Wire Nets to ac terminate the bus using a series resistor and capacitor connected to ground. After the capacitor charges, it blocks DC current so the series resistor presents no load to the bus. During transitions however, the capacitor appears as a short circuit and the resistor terminates the line. A general rule of thumb for selecting the capacitor, is 3 times the rise time divided by cable impedance. For a 4 microsecond rise time on 100 Ohm cable, this works out to be 0.1µF. The disadvantage of ac termination is the bit dependent timing jitter it generates due to the charging and discharging of the terminating capacitor shifting the waveforms.

Since it is not possible to terminate the ends of the cable in its characteristic impedance, the alternative is to control the slew rate of the bus master pull down transistor. For bus lengths of 100 meters or more a 1.1 volt per microsecond slew rate is recommended. This provides a one to zero transition

that takes about 4 microseconds to ramp to the 0.8V logic low threshold. Because port transistors in 1-Wire devices only hold the line down after the bus master pulls it low, they do not normally exhibit slew rate problems. The exception is when a Presence pulse is generated in response to a Reset command from the bus master since the slew rate of the Presence pulse of a 1-Wire slave is essentially uncontrolled. Disruptive edge rates also occur when a new 1-Wire device is connected to the net.

Phantom Presence pulse

If the net consists of a fixed collection of 1-Wire slaves, the slew rate problem of their Presence pulse can be overcome by generating a "Phantom Presence Pulse" with the bus master. This is simply an artificial slew rate controlled Presence pulse created by the bus master that starts at 10μS and terminates at 60μS. A sample pulse can then be generated at 70μS to see if a slave is on the bus or node if desired. This technique masks the high slew rate of the slaves high-to-low Presence pulse transition because the bus is already at logic zero when they occur. However, the Phantom Presence pulse technique is obviously ineffective with new slaves which arrive at unpredictable times on the bus.

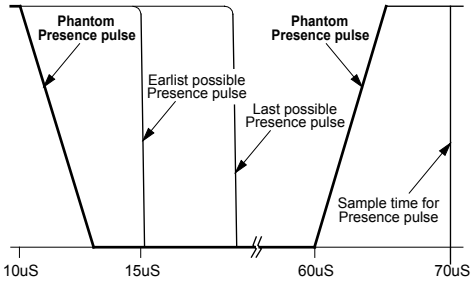

Figure 2 A Phantom Presence pulse can be generated by the bus master prior to any possible Presence pulse from a slave. It must last until the slowest possible Presence pulse has started.

Controlling the edge

Figure 3 shows a suggested slew rate control circuit. The 2N7000 shown, is a commonly available general purpose n-channel FET, but transistor characteristics are not critical and almost any general purpose n-type transistor may be substituted. A bipolar type such as the 2N2222 may also be used with minor component value changes to provide the recommended slew rate. Refer to the Appendix for additional information and a 1-Wire waveform template.

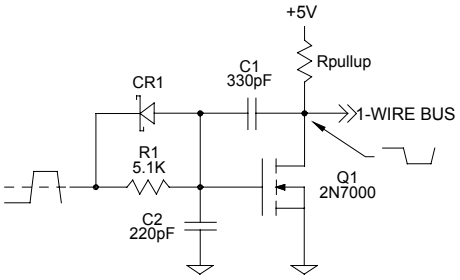

Figure 3 A controlled slew rate pull down for the 1-Wire net bus master. Transistor type is not critical.

Pulling up the line

Once both master and slave turn off, the bus pull-up resistor pulls the data line high. As the capacitive load on the net increases by adding 1-Wire devices, the time to raise the data line to the supply voltage also increases. This also occurs when the network is lengthened due to the 50pF of capacitance added per meter of twisted pair cable. This can be seen in **Figure 4** as the number of slaves is increased from 1 to 300. If the product of the total capacitive load (including cable, device, stray capacitance, etc.), and the pull-up resistor value results in a time constant (RC) that exceeds the bit time slot defined by 1-Wire

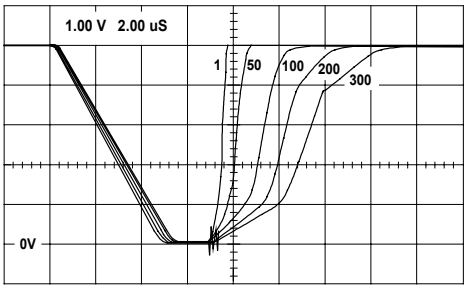

Figure 4 Loading effect of increasing the number of 1-Wire devices using active pull-up, and 2m cable.

protocol, communication stops. Because grounding unused wires or shields in a cable adds capacitance

which can significantly increase the RC time constant, they should be left disconnected.

As can be seen in **Figure 6**, the input capacitance of 1-Wire devices contribute to the capacitive load on the network. However, the 800 pF parasitic power supply capacitance only exists at voltage levels above 2.8V minimum. Ignoring the capacitance of the parasitic power capacitor, the bus pull-up resistor value, together with the cable capacitance and 1-Wire device input capacitance represent the network time constant τ. This is a reasonable omission since parasite capacitance does not become a factor until the bus has already passed the 2.2V logic one threshold. The network time constant determines the rate at which the data line returns to a logic one voltage. With the requirement that at t equals 13.02 microseconds (the original data sample time) the 1-Wire voltage needs to have reached the 2.2V threshold of a logic one, the value of τ can be calculated as follows.

$$\tau = 13.02\ \mu s / \ln (Vs/(Vs-2.2V)) = 22.4\mu s$$

Where Vs is the pull-up supply voltage. Using the recommended 1.5K minimum pull-up resistor value and 5V supply voltage, τ is calculated as 22.4 microseconds. Assuming the net is loaded with the maximum fanout as calculated in a later section, the cable capacitance alone must not exceed 12nF to yield a network time constant no more than the value just calculated. Using 50 pF/m for the typical cable capacitance implies that the theoretical maximum cable length is 240 meters. If the data sample time is recalculated with the new value of 21.7 microseconds, τ becomes 37.4µs. This permits 22nF of cable capacitance, which represents a cable length that exceeds the maximum allowed round trip propagation time. The effect of cable capacitance on the signal can be seen in **Figure 5**, where 100 1-Wire slaves were addressed at the end of a 2 and 100 meter cable. The 100 meter cable added 5000pF of capacitance.

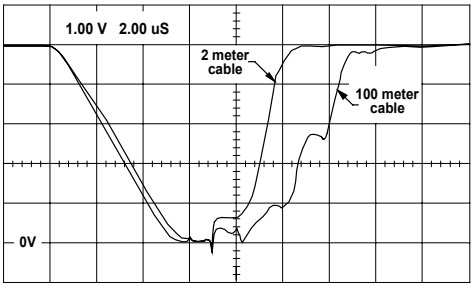

Figure 5 Effect of cable capacitance on signal driving 100 1-Wire devices. The 100m cable adds 5nF.

The risetime can be improved by reducing the value of the pull-up resistor, using lower capacitance cable, shortening the cable, or reducing the number of devices on the bus. The pull-up resistor, however, should not be reduced below 1.5 kΩ. Reducing the value of the pull up resistor increases the logic zero voltage on the network, reducing system noise immunity. If the value of the pull-up resistor is already minimum, an active pull-up may be substituted. This also allows use of longer cables by decreasing the network time constant. Of course, the same rules apply to an active pull-up as to a pull down, and slew rate must be controlled to avoid operating in a transmission line environment. The effect of residual current flowing in the bus when the active pull-up turns off can be seen in **Figure 8**. This was of little concern with a passive pull-up as an RC time constant has an inherently slow slew rate.

An active pull-up

One convenient source of an active pull-up is the MAX6314. This part was designed by MAXIM as a bi-directional open-drain µP reset for the 68HC11. However, it contains circuitry to automatically enable a 20mA p-FET pull-up for 2 microseconds when the data line exceeds a trip voltage of about 0.6V on the rising edge. Unfortunately, it does generate a logic zero output whenever the supply voltage drops below its reset threshold (it's intended use). For use on the 1-Wire net this can be detrimental as heavily loaded data lines can cause a reset, disabling communication, so selection of a part with a low reset threshold is suggested. One possibility is the MAX6314US31D3-T. This part has a 3 volt trip level that allows the supply to drop 2 volts before it

generates a reset. The MAX6314 comes in a four pin SOT143 package that requires little PCB area.

Although the MAX6314 contains an internal 4.7K pull-up resistor, it is recommended that an external 2.2K resistor be added in parallel. This provides the equivalent of the recommended minimum 1.5K pull-up resistor, which results in the bus crossing the trip voltage in minimum time. The bus waveform then exhibits three distinct segments. When both the master and the 1-Wire devices release the data line, it starts rising at a rate determined by the value of the pull-up and the total capacitive load (RC time constant). When it passes its trip threshold of approximately 0.6V, the 20mA p-FET is turned on and accelerates the bus toward the supply voltage. If the bus is heavily loaded, the 2 microsecond one-shot may time out with the bus well below the supply voltage. If this occurs, the 1.5K equivalent pull-up resistor continues to raise the bus voltage at the rate seen when the bus was first released. All three of these segments can be seen in **Figure 4**. This data however, was taken with a discrete proprietary design and not with the MAX6314. Refer to **Chapter 2** for additional information on active pull-ups.

The maximum voltage to which the bus pull-up resistor can raise the data line is determined by the product of the pull-up resistor value and the idle current of all devices on the line. The more devices, the greater the voltage drop across the pull-up resistor. The fanout limit of a particular 1-Wire net is reached as the voltage drop across the pull-up resistor reduces the net supply voltage to 2.8V. This is the minimum voltage that will recharge the parasitic power supply of the 1-Wire devices. From this, the maximum theoretical fanout may be calculated. It is equal to the supply voltage (Vs) minus 2.8V (the minimum operating voltage) divided by the pull-up resistor value. The resultant is divided by 15µA, the worse case device supply current. For a 5V supply and 1.5K minimum pull-up resistor value we have the following.

Fanout $_{MAX}$ = (5-2.8)/1.5K=1.47mA/15µA=98 devices

This represents the theoretical maximum number of 1-Wire devices that can successfully communicate with the master using a 1.5K pull-up resistor and 5V supply over worse case conditions of current and temperature. The assumptions being that all devices are drawing the maximum supply current and operating in a -40 to 85°C environment. In the real world, all devices will only be drawing the 15µA maximum supply current during System Reset and Presence Detect. At that time all device oscillators turn on for 5T times. Since 1T time typically lasts 30 microseconds, 5T times represents 150 microseconds, with a worse case of 255 microseconds. Circuit design ensures that all 1-Wire devices will be able to operate from their internal parasite power source for the duration of this interval once fully charged. Thereafter, they will be drawing 5µA maximum which permits tripling the previously calculated fanout of 98. In addition, most systems will be operating over a much narrower temperature range which allows still larger fanouts. For example, in a typical lab environment, over 500 1-Wire devices in continuous communication had only a 1.2V drop across the pull-up resistor. This implies that typical idle current per device is less than 2µA when environmental and supply ranges are limited.

SECTION 3
Its all in the cable

Take care in selecting a cable

As previously mentioned, the 1-Wire net consists of three segments, a bus master, the wiring and connectors and the 1-Wire slaves, as shown in the electrical equivalent circuit of **Figure 6**. The wiring between the master and the slaves is modeled by the inductance and resistance of the data and return lines and the lumped capacitance of the cable. Cable capacitance is simply the product of cable length times unit capacitance. This is typically 50pF/m for the recommended Category 5 twisted pair cable. Similarly, line resistance represents cable length multiplied by the specified resistance per meter of a single wire. A 1-Wire slave is modeled by its input capacitance (Cin), a constant discharge current (Idisc), the parasitic power supply circuitry (Di, Ri, Cload) and its operating current (Iop) of 10 µA during communication. The 5µA idle current per slave is required to keep its interface synchronized with the communication protocol. When the 1-Wire port transistor is on, its impedance is nominally less than 100 Ω, which provides a 0.4V logic zero with a 4mA current sink. If multiple 1-Wire devices are residing

on the bus, Cin, Idisc, Iop and Cload should be multiplied by the number of devices to determine the total. Ri needs to be divided by the number of devices. The port transistor inside the slave allows it

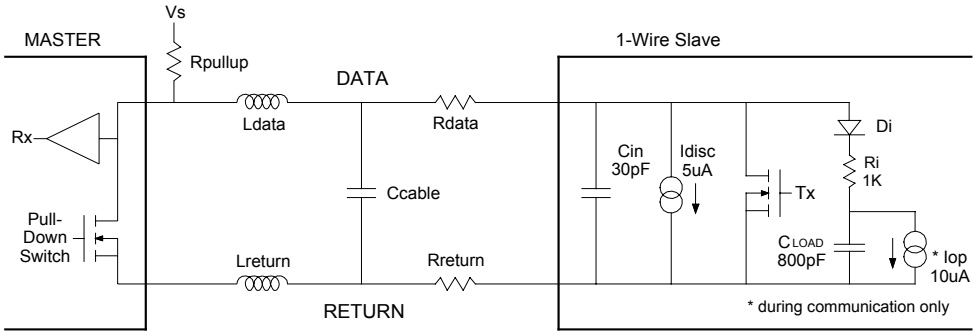

Figure 6 Electrical Equivalent Circuit of the 1-Wire net

to place a logic zero on the network. Except for the presence detect cycle, Search, Skip and Read ROM commands, only one of them will be conducting when addressed by the bus master.

While parasitic resistance reduces the zero logic level noise margin of the digital signals, cable capacitance together with the parasitic power supply of 1-Wire devices adversely affect the size of the network. At power up, this capacitive loading can require several milliseconds to charge before communication can start on the net, especially if a passive (resistive) pull-up is used. Also on long lines with many slaves grouped at the end, the parasitic power requirements create a dip or slope change in the rising edge of the waveform at about 2.8V as the energy reservoirs of the devices are filled. Once full, the recovery time after each time slot will be sufficient to maintain the charge. **Figure 7** shows the effect charging the parasite power capacitance has on different numbers of 1-Wire devices at the end of 100 meters of Category 5 cable. Notice that the slope of the rising edge decreases as it crosses the 2.8V threshold finally reversing direction to form a dip when loaded with 100 or more devices. These “dips” become more pronounced the longer the bus remains low.

Clearly the physical properties of the cable connecting the master and 1-Wire slaves strongly dominates the network. Comparison of the waveforms shown in **Figure 4** taken with two meters of Category 5 cable to those of **Figure 7** taken with 100 meters makes this plain. For short runs up to 30 meters, cable selection for use on the 1-Wire net is less critical as the impedance characteristics are generally insufficient to have a marked adverse effect on the bus. Even flat modular phone cable works with limited numbers of 1-Wire devices. However, the longer the net, the more pronounced cable effects become, and consequently the greater the importance placed on cable selection.

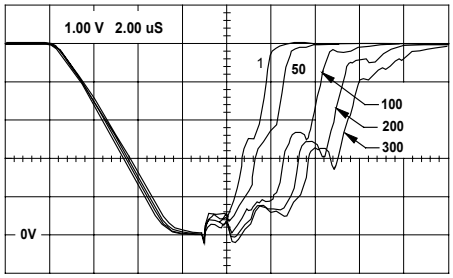

Figure 7 Parasite power loading of 0 to 1 transition. Notice that the dip becomes more pronounced with increasing number of devices at end of 100m cable.

Given sufficient length, any cable exhibits transmission line effects. Real cables display distinct properties of resistance, capacitance and inductance, which in turn are determined by cable geometry, the size and spacing of the conductors and their surrounding dielectric. These physical properties define the characteristic impedance, the signal bandwidth supported and the propagation

velocity of the cable. Specifically, cable resistance reduces the zero logic level noise margin, although values to 100 Ohms for the total cable length are acceptable. Cable capacitance however, which can range from 30pF/m to 100pF/m, loads the 1-Wire net driver, increasing not only the network time constant (τ) computed earlier, but also the peak current flowing in the cable as the bus pull down transistor turns on and discharges the line.

If this transistor turns off before the charge stored in the line capacitance is completely discharged, the residual current left flowing in the line determines the amplitude of a transient voltage spike generated as a product of this current and the cable inductance. The resulting voltage spike seen at the driver can become large enough to interfere with communication. The effect of residual current flowing in the cable when the bus pull down transistor and the active pull-up turns off can be seen in **Figure 8**. Notice that in each case, the spike generated is in the direction of the opposite rail. At the far end of the cable, when the pull down transistor turns off it's inductively

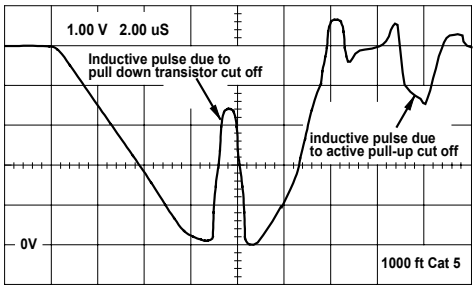

Figure 8 Inductively generated voltage spikes such as seen here, can occur on long lines due to residual current flow when pull down or pull-up circuits turn off.

generated voltage spike swings negative, reverse biasing the substrate of the 1-Wire device closest to the cable end which clamps the voltage excursion at a diode drop. This device will then not respond to the bus master.

The problem is differential inductance, which is measured across the cable input with the line shorted together at the far end. Differential inductance is substantially lower than the inductance of a single wire because the current flows in opposite directions in the pair and in the ideal case would cancel completely. Because differential inductance decreases as the distance between conductors is reduced, use of adjacent and preferably, twisted pair is recommended. Twisted pairs help reduce unwanted coupling from nearby interference sources because the currents induced in the two wires flows in opposite directions and tends to cancel.

Another concern is that the recommended category 5 unshielded twisted pair cable is commonly available with multiple pairs. While the capacitance between wires in a single pair is approximately 50 pF/m; that between wires of different pairs is closer to 30 pF/m. Because grounding the unused wires will add this 30 pF/m to the 1-Wire capacitive load, unused wires and shields need to be left unconnected at both ends of the cable. Grounding them can increase the capacitive load to the point that the bus pull-up cannot raise the line above the logic switching threshold within the bit time slot and communication stops. Refer back to Section 2 and the discussion of network time constant in "Pulling up the line" for more information. It is also not recommended to simultaneously run two 1-Wire nets in the same cable bundle, because the capacitive load varies dynamically dependent upon data pattern, which can lead to erratic operation.

Keep the bus running

As line inductance increases, the product of L di/dt can generate voltage excursions that cause bit errors and reverse bias the substrate of at least the first 1-Wire device at the far end of the cable. These voltages spikes are generated by the current still flowing in the data and return lines of the cable when the transistor in the master is turned off before the charge stored in the line capacitance is fully discharged. The obvious and recommended solution is to maintain the pull down transistor in the on state until the current in the line discharges. If it is not possible to stretch the timing, a Schottky diode placed across the bus at the far end is suggested to clamp the inductive generated voltage overshoot. Connect the diode across the cable with the cathode on the data line and the anode on the return. Only one diode is required for each branch.

SECTION 4
Rewiring the LAN

The DS2409 MicroLAN Coupler

Historically, the 1-Wire net was envisioned as a single twisted pair routed throughout the area of interest with 1-Wire slaves being attached in a daisy chain fashion where needed. However, if the network is heavily loaded, and/or very long, it may be preferable or even necessary, to separate the bus into sections. This has the added benefit of providing information about the physical position of a 1-Wire device on the bus which facilitates trouble-shooting. By using one section as the main "trunk", and adding or removing segment "branches" to it with a DS2409 as needed, a true 1-Wire net is created. It is also possible of course to add or remove additional segments to the branches using a MicroLAN Coupler as the node control. This approach reduces the capacitive and idle current loads the bus master sees to that of the trunk and those segments connected to it by activated DS2409's. However, the limitations to the total capacitive load, idle current and line length covered in earlier portions of this document still apply. That is, for the trunk and activated sections of the LAN, the capacitive load must be low enough to allow the bus pull-up to raise the line above the logic one threshold within the time slot. The combined idle current of the 1-wire devices must not reduce the supply voltage below 2.8V. And the electrical length of activated cable must allow a transition from the master to reach the cable end and return within the time slot.

The DS2409 MicroLAN Coupler is a key component for creating complex 1-Wire nets. It contains the MAIN and AUX transmission gate outputs, plus an open drain CONT output transistor, each of which can be remotely controlled by the bus master over the 1-Wire network. Both the MAIN and AUX outputs support a "smart-on" command which generates a reset/presence sequence on the selected output before connecting to the 1-Wire bus. This allows a subsequent ROM function command to apply only to the devices on the just activated segment. The main caution is that the DS2409 requires a 5V supply without which it shorts the 1-Wire bus and no communication is possible. Since the DS2409 contains no user available memory, the AUX output can be used to label the node by connecting a 1-Wire memory chip to store the required data. A simple 1-Wire net branch with EEPROM labels connected as described is shown in **Figure 9**. Tagging protocol information is available on the Dallas Semiconductor ftp site at ftp://ftp.dalsemi.com/pub/auto_id/softdev/softdev.html.

In the example, a DS2430 EEPROM is connected to the DS2409 AUX output. This provides tagging information specific to that particular node such as location, function, etc. The LED attached to the CONT output provides visual indication of the specific branch being addressed and can be caused to flash via software for extra visual impact. A single DS1820 Digital Thermometer is shown on the branch output but multiple 1-Wire devices can be placed as required.

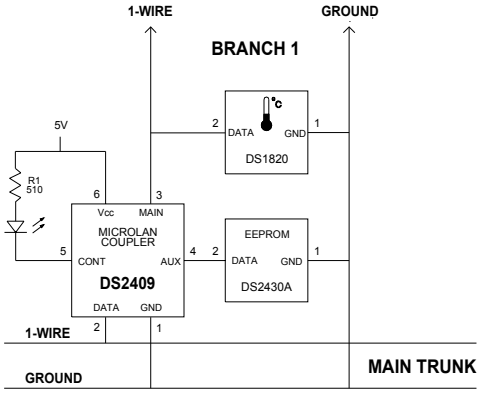

Figure 9 Separating the 1-Wire bus into branches using the DS2409 MicroLAN Coupler.

To avoid loading the entire 1-Wire net with the capacitance associated with routing power along with the 1-Wire DATA and GND, the CONT output of the DS2409 can be used to operate a pass gate transistor to switch the 5V supply along with the MAIN output switching the branch. The MICREL MIC94031 transistor shown in **Figure 10** contains the gate pull-up resistor shown, so implementing the circuit requires only the addition of a single SOT-23 package. By default, whenever the MAIN output of the DS2409 is turned on, the CONT output is pulled low, turning on the pass gate and routing power to

the selected branch. Turning MAIN off automatically turns CONT and therefore the pass gate off, so no software revisions are required for the circuit. The DS2409 is available in a 6 pin TSOC surface-mount package. For further information about the DS2409, refer to the datasheet available on the Dallas Semiconductor website at www.dalsemi.com.

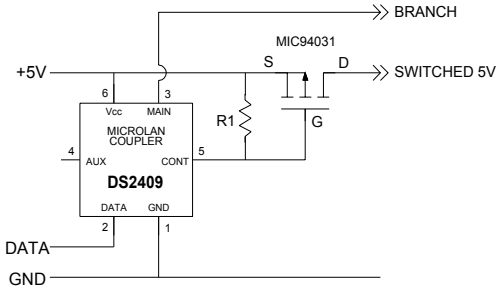

Figure 10 Method of switching local power to a branch using a DS2409 and a pass transistor.

The DS2406 dual addressable switch

The DS2406 is a low side addressable switch intended for remote control perhaps in combination with an opto-coupler or relay; or to provide visual indication of an operation or end-of-limb by means of an LED (Light-Emitting-Diode). The DS2406 is **not** recommended as a means for providing branches on a 1-Wire net, because branching requires use of a high side switch. This is because current flowing through the on-resistance of the port transistor develops a voltage that raises the ground pin of all devices connected to it above the ground reference. Since the 1-Wire slaves will be hard wired to the data the potential on the data pin becomes negative with respect to the voltage on its ground pin. This polarity acts to forward bias various p-n junctions in the slaves resulting in device dependent disruptions. For example, when this voltage reaches approximately negative 0.3V, it can continuously activate the POR (power-on-reset) of any attached DS2406, effectively removing it from the bus.

The DS2406 addressable switch was designed to perform closed-loop control of its two open drain output transistors, PIO-A and PIO-B, over twisted pair cable up to 300 meters from a PC. Each output can also sense and report to the PC the logic level at its port. When turned on by the bus master, the PIO-A port is connected to the IC ground pin and can sink up to 50 mA, and hold off a maximum of 13V, while the PIO-B sinks 8 mA and holds off 6.5V. The on-resistance of the DS2406 PIO-A output transistor is about 10 Ohms, whereas the PIO-B output is about 50 Ohms. The off impedance of both addressable switches exceeds 10 Meg Ohms. The DS2406 is available in a 6 pin TSOC surface-mount package, or as a single channel (PIO-A) version in a TO-92 package. For more information on the DS2406 dual addressable switch which contains 1K of one time user programmable EPROM, refer to the datasheet available on the Dallas Semiconductor website at www.dalsemi.com.

Using both the high and the low switch

While the DS2409 and DS2406 are very useful when used alone, together they can form the basis of a general purpose Pick system. **Figure 11** shows two DS2409s being used to select an arbitrary row, while a dual DS2406 low-side switch is used to select an arbitrary column. As shown, they form a simple 2X2 array with LEDs to visually indicate the specific intersection being addressed by the bus master. However, the array can be easily expanded in either the X or Y direction by the addition of more DS2409s and/or DS2406s. In this manner an M by N array of any required size may be implemented limited only by net loading.

In operation, the master selects the Aux output of the DS2409 that controls the row of interest, and the column output of the corresponding DS2406 that intersects that row at the required position. For example, if the AUX output of the top DS2409 and the B output of the DS2406 are both turned on, the position in the upper right hand corner is selected. This connects the iButton port at the intersection of the selected row and column to the master so the serial number of the 1-Wire device (if any) at that point can be read. To indicate which intersection is being addressed, the master switches the selected DS2409 from its Aux output to its Main output. By default this causes the CONT pin to turn on, grounding the gate of the associated pMOS transistor and turning it on. With the pass transistor on, power is supplied to the LED at the selected intersection and turns it on. If desired, the DS2409 can be switched repeatedly between Main and Aux causing the LED to blink for greater visual effect. If

the Main outputs of all DS2409s are turned on, the LEDs in the entire column of the selected DS2406 turn on. Alternatively, if the outputs of all DS2406s are turned on, the LEDs in the entire row of the selected DS2409 turn on. Consequently, it follows that turning on all column and row switches illuminates the entire array which serves as a convenient test to verify that the system is fully functional. While an iButton port was shown in the example, a blue-dot connector or even solder mount devices could be substituted.

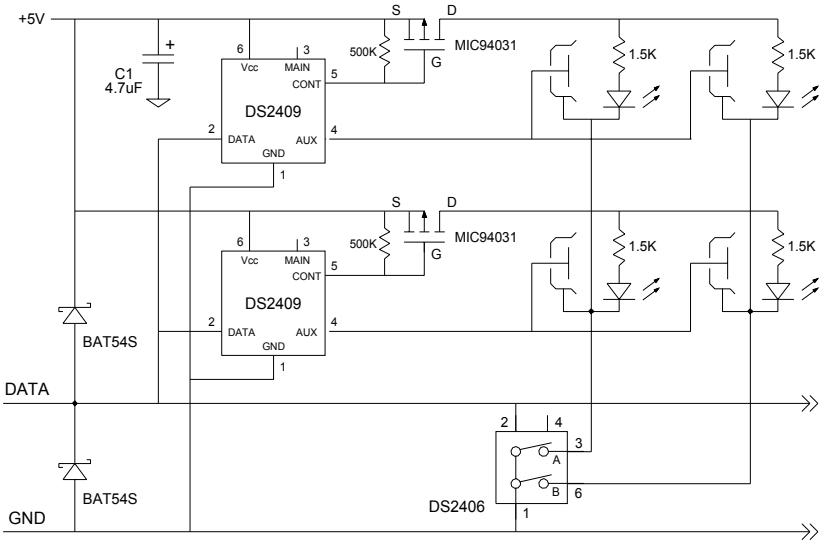

Figure 11 Using DS2409s and DS2406s to form an X Y matrix Pick system with visual indicators.

SECTION 5
Policing the LAN

Protection and Noise

All 1-Wire net compatible devices contain built-in ESD (electrostatic discharge) protection circuitry able to withstand ± 10kV minimum Human Body Model ESD events. However, when interfacing a computer to a 1-Wire net it is good engineering practice to provide additional means to protect the system from ESD and EMI (electromagnetic interference) damage. Economical protection can be provided at the bus master by means of diodes that short negative spikes or shunt positive ones higher than 5V to the power supply bus where they are absorbed by capacitors and other protection devices. When selecting protection diodes or surge suppressers, choose devices with minimum junction capacitance and fast switching times. Two good examples are the ERA82 Schottky diode from FUJI or the multi-source 1N5817. The BAT54x series of Schottky diodes available in the SOT-23 surface mount package is also acceptable. Refer to **Figure 11** for an example using the BAT54S dual diode.

If 1-Wire EPROM parts will not be programmed using the RS232 to 1-Wire interface adapter, excellent protection can be provided with a single DS9502 ESD protection diode. These behave like a 7.5V zener diode during normal operation, however, if the voltage across them exceeds their 9V trigger voltage they fold back to 5.5V. If exposed to an ESD event beyond their ratings, the DS9502 will eventually fail shorted, preventing damage to the protected circuitry. The DS9502 is available in a 6 lead TSOC package, or as a CSP solder mount “bumped” die.

Introducing the DS2480

In order to reduce the engineering load of setting up a 1-Wire net, Dallas Semiconductor has developed the DS2480 Serial 1-Wire Driver. This IC connects

directly to UARTs and 5V RS232 systems. Adapters are available using the DS2480 that connect directly to a standard COM port and provide 1-Wire outputs. The IC contains programmable pull-down slew-rate control and an active pull-up. Other features include support for data rates of 9.6 (default), 19.2, 57.6 and 115.2 Kbps and programmable 1-Wire timing. The DS2480 is available as the DS9097U-x09, which is a DB9 to RJ11 COM port adapter, and the DS1411 with a DB9 to DS9098 iButton socket. These are true ground Crypto-capable adapters with FCC class B approval. A schematic of the DS9097U is provided in Chapter 2.

Its the results that count

By applying information presented in this application note such as using Category 5 twisted pair, controlling slew rates and substituting an active pull-up, reliable communication over 300m of cable with more than 500 assorted 1-Wire devices was demonstrated. Without slew rate control and active pull-up, the limit is about 100 meters with 150 1-Wire devices.

Recommendation summary for operating long or heavily loaded MicroLANs:

Select cable

- Good -twisted pair phone
- Better -Category 5 twisted pair

Use a diode clamp

- Use a Schottky diode across the cable's end. Connect the diode reverse biased with the cathode on the data line and anode on the return.

Use multilevel branching

- Use DS2409 MicroLAN Couplers to separate the net into branches.

Use a DS2480 based COM port adapter

- a DS9097U-009, a DB9 to RJ11 adapter
- **or a**
- DS1411, a DB9 to DS9098 socket adapter

If a DS2480 type adapter is <u>not</u> used,

Control slew rate

- Limit the slew rate of the pull down to about 1.1 volts per microsecond.

Use an active pull-up

- Replace the pull-up resistor with an active pull-up, limiting slew rate to about 1 V/μS.

Keep the bus running

- Keep the bus master transistor on until residual line current dissipates.

Use later sampling

- Use 21.7 microsecond timing (2.5T), instead of the original 13.02 microsecond (1.5T) timing.

CHAPTER 2
Hardware for the 1-Wire net

PC to 1-Wire net adapters

Any PC with a UART capable of 115.2 kbps can serve as bus master for reading and writing 1-Wire devices on the net. However, a serial COM port to 1-Wire adapter is needed to interface the computer RS232 levels to the 5V 1-Wire bus. A schematic for the original DS9097 COM port adapter developed by Dallas Semiconductor as an economic and easy to use interface, is shown in **Figure 12**. The adapter is powered entirely from the computer COM port. Note that the circuitry makes maximum use of the UART controlled output using only clamping and level shifting diodes. Although this provides a simple and reliable circuit that directly couples to the serial port, it lacks a ground reference. While not of concern in operating the net, it can present complications during trouble shooting, as the oscilloscope ground cannot be connected to the 1-Wire return. Connecting the DS9097 1-Wire return to ground can result in permanent damage to the adapter.

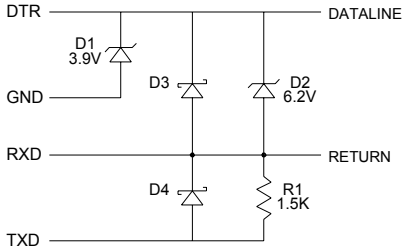

Figure 12 The DS9097 COM port adapter. Note that "return" is not ground. R1 is the bus pull-up.

In **Figure 12**, current limiting and slew rate control are provided by the UART as RS232 requirements, while zener D1 clamps the data line at 3.9V. Zener diode D2 limits the maximum voltage range on the 1-Wire bus to 6.2V. It also restricts the most negative voltage swing on RXD to minus 2.3V. When TXD is positive, Schottky diode D3 limits the voltage difference between the 1-Wire data and return lines to 0.2V, and D4 connects TXD to RXD. This bypasses R1 the passive bus pull-up, and provides a low impedance path to initiate a time slot. The 1.5K minimum value pull-up resistor generates a 0.3V logic zero across the 100 Ohm on-resistance of a 1-Wire device. Since the maximum voltage still recognized as a logic zero is 0.8V, this leaves 0.5V of noise margin.

The DS9097 comes with a DB9 for attachment to a PC serial port and an RJ11 for connecting to the 1-Wire net. The same circuitry is available in a DB9 to DS9098 socket as the DS1413. A DS9097E version in a DB25 case is also available for programming EPROM based 1-Wire products such as the DS198x series. It provides a power jack to accept an external 12V auxiliary supply as required.

A true ground COM port adapter

If the return line of the net must be grounded at some point, a true ground COM port adapter interface is required. The schematic for a true ground adapter is given in **Figure 13**. Its positive supply is derived from DTR and RTS by Schottky diodes CR1 and CR2, and filter capacitor C1. A well-regulated 5 volts is provided by the low dropout LP2980 voltage regulator as long as the COM port provides at least 5.1V. If the positive level of both DTR and RTS drops below this the regulator drops out of regulation. CR3 and C3 provide the negative supply required by the DS275 RS232 Transceiver chip from TXD during read data and idle time slots. The DS275 connects directly to the 1-Wire net converting it's CMOS/TTL levels to the RS232 levels required by the UART. If surface mount components are used, the circuitry will fit comfortably on a 0.6" by 0.9" printed circuit board. This can be mounted inside a DB9 female to RJ11 PC adapter.

A slew rate controlled pull down

Because it is not possible to terminate the end of the cable in its characteristic impedance, the alternative is to control the slew rate of the bus master pull down transistor to prevent adverse transmission line effects. For more information on this subject, refer back to Chapter 1 and "Control the slew rate of the driver." In **Figure 13**, transistor Q1 and the components associated with its gate, limit the slew rate to about 1.1 volts per microsecond. This provides a one to zero transition that takes about 4 microseconds to ramp from the 10 to 90% points. This has proven to be adequate for cable lengths exceeding 300 meters. The 2N7000 shown is a commonly available general

purpose n-channel FET, but transistor characteristics are not critical and almost any general purpose n-type transistor may be substituted. A bipolar type such as the 2N2222 may also be used with a base resistor and minor component value changes to provide the recommended slew rate.

In the pull down circuit of **Figure 13**, Miller integrator capacitor C5 across Q1 acts as the primary slew rate control element. On lightly loaded LANs using about 50 devices on 50 meters or less of cable, it may be possible to eliminate C5. Sufficient slew rate control is then provided by R1 and C4. In operation, when TXD switches from its minus 12V rail to the plus 12V rail, the signal is passed to the gate of Q1 by input resistor R1. This transition is slowed and delayed slightly by the RC time constant of R1 and C4. When the voltage level at the gate reaches the threshold voltage of Q1, the transistor begins to turn on. The effect of the transistor turning on with C5 across its terminals results in a nearly linear voltage ramp from the supply voltage to ground. This one to zero transition on the bus is the synchronizing edge for 1-Wire communications. Q1 remains in the on state for the duration of time that TXD is held at plus 12V by the UART. Afterward, the bus is returned to the supply voltage by the action of pull-up resistor R2. Zener diode D1 serves several functions in the circuit. It protects the gate of Q1 by limiting positive voltage excursions to 12V, and negative ones to minus 0.6V. Gate input resistor R1 limits the current through the zener. The capacitance of D1 also adds to that of C4, helping control the transistor transition.

While they are not shown for clarity reasons, good engineering practice would place reverse biased Schottky diodes across the output of the circuit. One diode should be from the supply voltage to the data line, the other from the data line to ground. Use of ultra fast low capacitance Schottky diodes such as the 1N5817 or the ERA82 from FUJI is suggested. The BAT54x series available in SOT-23 packages is also acceptable.

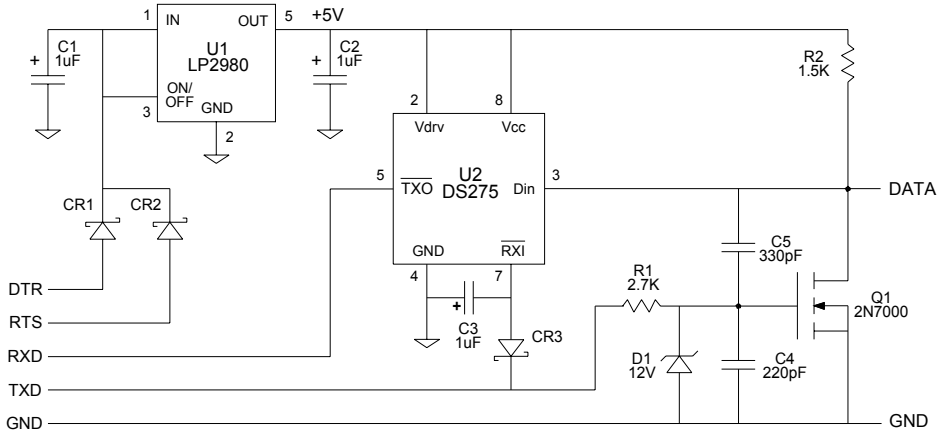

Figure 13 A PC serial COM port to 1-Wire net true ground adapter. Q1 is the slew rate controlled pull down and R2 is the passive bus pull-up resistor.

So that's how it works!

A cycle in the sequence of 1-Wire net communication over the true ground COM port adapter would proceed as follows. Initially, TXD would be at minus 12V (an RS232 "mark" or logic one), so the gate of Q1 would be clamped at minus 0.6V by the reverse bias on zener diode D1. Consequently Q1 is off, and the bus will have been raised to the 5V supply by pull-up resistor R2. When TXD switches between the minus 12V and plus 12V rails, Q1 will be turned on and ramp the bus voltage down at the rate set by the Miller integrator capacitor C5. This one to zero transition has two paths, one continues down the bus, the other returns to the UART through U2. The

signal returned to the UART, will be used to determine when to reexamine its registers for a response from a 1-Wire device on the bus.

Meanwhile, the transition traveling down the bus is received sequentially by any attached 1-Wire slaves as the edge propagates past them. If this signal from the UART is a Reset pulse, it lasts for at least 480 microseconds and then releases the bus. The bus pull-up raises the line to the supply, and approximately 30 microseconds later the UART reexamines its registers to see if a Presence pulse is being sent by a 1-Wire device. In the interim, the internal oscillators and controllers within each 1-Wire device have determined that a Reset has been sent and at the appropriate time will pull the bus low. The exact time the bus is pulled low and its duration, is a function of individual device variation. The fastest will pull the bus low first, and the slowest release it last. When the final 1-Wire device releases, the pull-up resistor raises the bus toward the supply voltage at a rate determined by its value times the capacitive load it sees on the line (RC time constant). If the pull-up cannot raise the bus above the logic one threshold within the time slot, the master will always see a logic zero and conclude the line is shorted. Consequently, communication cannot occur. Assuming however that the timing is acceptable, the UART sees a proper Presence pulse indicating there are 1-Wire devices on the bus. It then proceeds to call serial numbers to identify them.

In order to write logic one or zero values onto the bus, the UART turns on Q1 for short (less than 15 microseconds), or long (greater than 60 microseconds) time slots respectively. To read, the UART begins by turning on Q1 for a short time slot exactly as if a logic one was being sent. If this time slot remains unchanged, the UART defines this as reading a logic one. If a 1-Wire slave extends the time slot initiated by the master by continuing to hold the line low (even though the UART has released Q1 and R2 attempts to pull the data line high) the UART defines this as reading a logic zero.

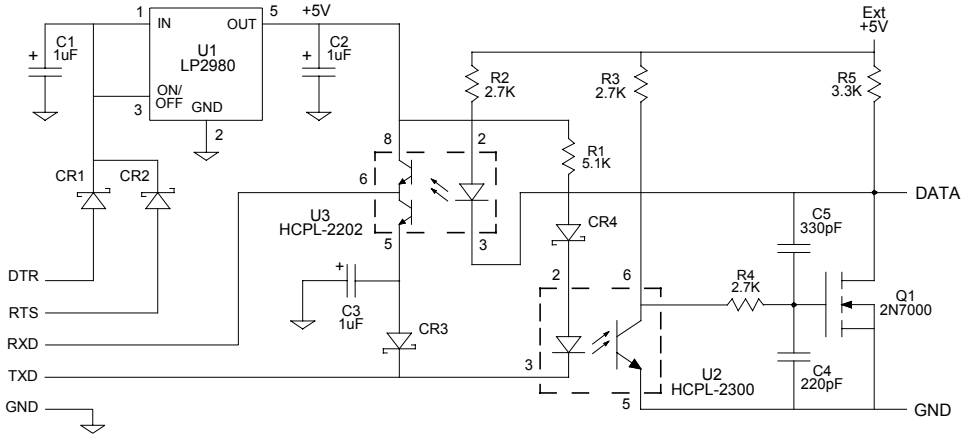

Figure 14 An optically isolated COM port to 1-Wire net adapter.

An optocoupler isolated adapter

In some applications, for safety reasons or because of ground loops, it is necessary to provide galvanic isolation between the computer master and the net. For such cases, the optically coupled adapter circuit in **Figure 14** is suggested. Optical isolation of the COM port requires special purpose optocouplers, such as the high speed, low input current HCPL-2300 used in the transmit section. An HPCL-2202 with 20V totem pole output is used in the 1-Wire to RS232 channel.

The HCPL-2300 has an 0.5mA input LED, and an output transistor with 200 nanosecond maximum

propagation time. In the circuit, the LED current is set with resistor R1, but a current source such as the J503 or CR056 from Siliconix will provide superior performance over the diversity of logic levels available with RS232. If a constant current source is not used it may be necessary to recalculate the value of R1 to maintain 0.5mA with the voltages in use on a particular RS232 COM port. CR4 is required to protect the LED, which only has a 5V breakdown in the reverse direction.

In operation, the HCPL-2300 coupler U2, provides the necessary isolation and level shifting from the double rail plus and minus 12V RS232 to the single rail 1-Wire net. The coupler is connected as non-inverting, so when TXD is at minus 12V, the LED input is on. Consequently, the coupler output transistor is also on and the bus pull down transistor Q1 is off. With Q1 off, bus pull-up resistor R5 holds the LAN at the supply voltage. U3, the receive optocoupler is also off, so its output is at minus 12V.

When TXD changes state, the HCPL-2300 input LED is reversed biased, turning the coupler output transistor off. Its collector is then pulled high by resistor R3. This zero to one signal is slowed and delayed slightly by the RC time constant of R4 and C4. When the voltage level at the gate reaches the threshold voltage of Q1, the transistor begins to turn on. The effect of the transistor turning on with Miller capacitor C5 across its terminals results in a nearly linear voltage ramp from the supply voltage to ground. When Q1 pulls the data line to ground, it also turns on the LED in U3 the HCPL-2202 coupler, causing its totem-pole output stage to switch to plus 5V. This transition will be received by the UART and used to determine when to reexamine its registers for a response from any 1-Wire devices on the bus.

The data line remains at ground until TXD returns to its original state, and Q1 along with any 1-Wire slaves turn off. At that time, the bus pull-up resistors (R5 in parallel with R2) raise the data line toward the 5V supply at a rate determined by their equivalent value times the capacitive load seen on the line (RC time constant). This turns off the input LED of U3, and causes its output stage to switch to the minus RS232 voltage level. Assuming the pull-up can raise the bus above 2.2V within the time slot, the UART will see a logic one, and communication proceeds. If the pull-up cannot raise the bus above the logic threshold within the time slot, the master will always see a logic zero and conclude the line is shorted. Consequently, communication stops.

An active pull-up

On a 1-Wire net where the minimum acceptable pull-up resistor value cannot raise the data line above the logic one threshold within the time slot, an active pull-up must be used. Obviously, an active pull-up circuit should be on only during a defined range of the rising edge (zero to one transition). Conversely, it should not respond on the falling edge, nor be active during logic zero time intervals. It must trigger on the rising edge at about 0.9V plus or minus 0.1V to provide acceptable noise margin. Preferably, once triggered it will remain on until the line is raised above a specified threshold ($\geq$3V) rather than for a set time interval (one shot). This insures that the data line will be raised above the 2.8V level required to recharge the parasite power capacitors regardless of load. The maximum current supplied should be limited to about 15mA. Larger currents when flowing in cable inductance can cause problems. Refer to Chapter 1 Section 3 “Its all in the cable” and see **Figure 8** for more information on the effects of cable inductance.

In Chapter 1 Section 2 under “An active pull-up," use of the MAX6314 is suggested as an available circuit. This part was designed by MAXIM as a bi-directional reset intended for use with the 68HC11 microprocessor. As such, an important function of the chip is to monitor the supply voltage and assert a reset (logic zero) during power-up, power-down, or during supply droop. This obviously is an undesirable function on the net. However, the part includes an active pull-up to solve the RC time constant problem faced on a high capacitance bus. Coincidentally, this consists of a p-FET in parallel with a 4.7K pull-up resistor (the maximum 1-Wire net value). The FET is turned on for 2 microseconds when the waveform on the reset pin exceeds 0.9V maximum by a comparator triggered one-shot. Additional control circuitry ensures that the active pull-up is disabled at all other times.

Operation of the MAX6314 when connected to the 1-Wire net proceeds as follows. When the bus (connected to the MAX6314 reset pin) is pulled below 0.5V by the master, a comparator sets an internal flip-flop enabling the active pull-up control circuitry. When the bus is released, the internal 4.7K pull-up resistor starts raising the bus toward Vs (the bus supply voltage) at a rate determined by it's RC time constant. This generates a ramp that starts at the logic zero level and ends at the trip voltage of a

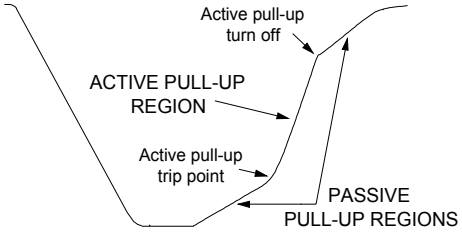

Figure 15 Characteristics of an active pull-up.

comparator. When the trip voltage of the active pull-up enable comparator is exceeded, it triggers a 2 microsecond one-shot that turns the 20mA p-FET on. This starts a second much steeper ramp that begins at the comparator trip voltage and ends at Vs. However, if the bus is heavily loaded, a third ramp may be created if the 2 microsecond one-shot times out, and the bus voltage has not reached Vs. This ramp starts where the one-shot times out, and ends at the maximum voltage to which the passive pull-up can raise the line with the idle current load of 1-Wire devices on the bus. This third ramp will have a slope similar to the first. The characteristic waveform produced by an active pull-up is illustrated in **Figure 15**.

Although the MAX6314 contains an internal 4.7K pull-up resistor, it is suggested that an external 2.2K resistor be added in parallel. This yields the equivalent of the recommended 1.5K minimum pull-up resistor, and allows the bus to cross the enable trip voltage of the active pull-up in minimum time. The combination of the MAX6314 and 2.2K resistor can be substituted for R2 in **Figure 13** to provide a true ground COM port adapter with active pull-up.

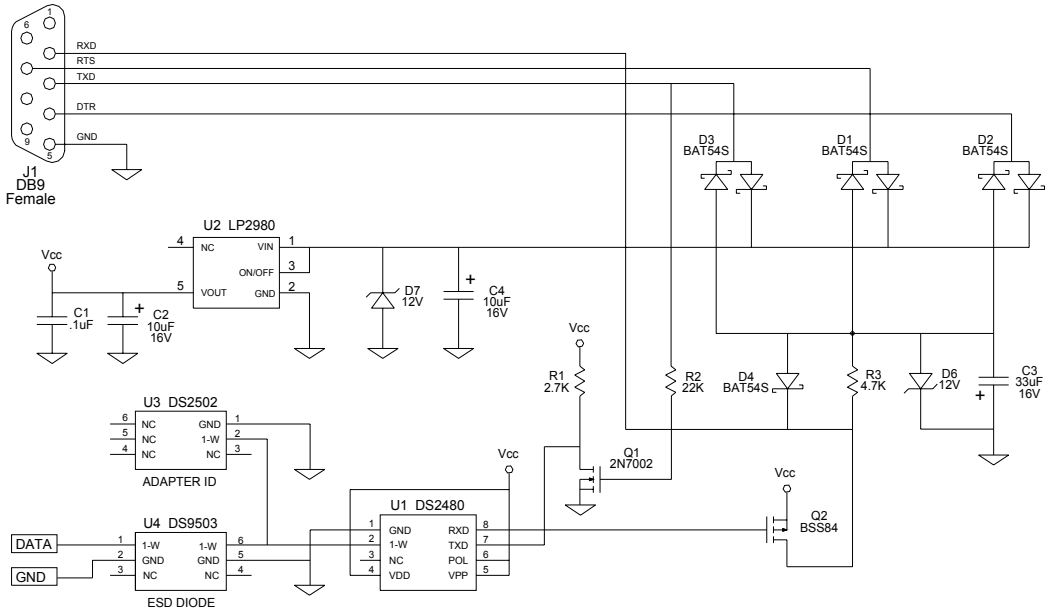

Figure 16 The schematic for the DS2480 based DS9097U COM port Adapter.

In order to reduce the engineering load of setting up a 1-Wire net, Dallas Semiconductor developed the DS2480 based series of COM port adapters. The basic schematic shown in **Figure 16** is used through-

out the series, the major difference being the type and number of 1-Wire connections on the output. The DS2480 provides programmable slew-rate control on the pull-down and an active pull-up. Other features include support for data rates of 9.6 (default), 19.2, 57.6 and 115.2 Kbps and programmable 1-Wire timing. The DS2480 also provides a strong pull-up mode to facilitate the higher current requirements of devices such as the DS1820 temperature sensor during conversion. The DS2502 shown is used to provide the adapter ID.

The DS2480 is available with and without an ID in a DB9 to RJ11 COM port adapter as the DS9097U-009 and DS9097U-S09 respectively. The circuitry is also available as the DS1411 with a DB9 to DS9098 iButton socket. All adapters are true ground Crypto-capable adapters with FCC and CE approval.

CHAPTER 3
Supplying power on the 1-wire net

1-Wire chips get both their power and communications over the same line making installation very economical. When adding power-consuming devices to the 1-Wire node, the same line can also supply power to them using one or more of the techniques described here. Typical examples could be as simple as driving an LED or operating a solenoid, or as complex as powering a pressure sensor. In such cases, the most convenient method would be to transfer the energy they require over the same communication line. This chapter will review some methods for providing power on the net including a technique for accumulating low level energy and releasing it on demand as a high energy burst.

In general, solutions to the problem of supplying power on the 1-Wire line fall into one of the following four methods. Keep in mind that regardless of which method is chosen, consideration must also be given to the energy required, its duration and its distance from the bus master.

- Sourcing power whenever the line is above 3.5V.
- Sourcing power by transferring charge to a capacitor through a blocking diode.
- Sourcing power with a strong pull-up during idle communication time.
- Alternative power source using additional wires and connections.

Tap the power between 3.5 and 5V

Because 1-Wire devices can operate with as little as a 3V supply, the energy available between the bus supply levels of 3.5 and 5 volts can be tapped. This is equivalent to operating the load in shunt mode and can be used to operate clamp type loads such as LEDs. This requires that the total voltage drop across the LED(s) be at least 3.5V. While it is possible to connect the shunt load permanently across the bus, preferably, the load would be operated under bus master control by connecting it between the 1-Wire DATA lead and the output of an addressable switch as shown in **Figure 17**. In this mode, 1-Wire communication takes place below 3.5V and power delivery occurs above that value. Whenever the output of the DS2406 is pulled low the LED is on and the voltage on the bus is approximately equal to 3.5V, the forward voltage of the LED. When the output is turned off, the LED is off and the bus voltage is at its nominal 5V value. Operational current is supplied by the bus master which for the DS2480 based DS9097U COM port adapter is normally limited to about 5 milliamps, but increases to about 15 milliamps when the active pull-up turns on. As shown in **Figure 17**, the bus voltage will be clamped to a level which keeps the active pull-up on and supplying 15 milliamps. A current limiting resistor connected between the DATA line and the LEDs will allow the active pull-up to turn off.

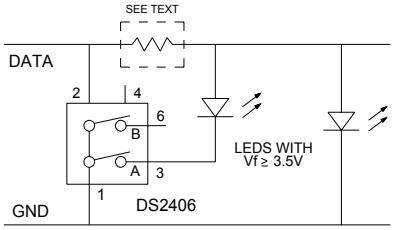

Figure 17 Using the power available between 3.5 and 5V directly and under bus master control.

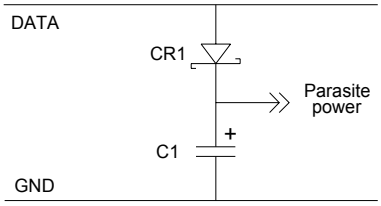

Figure 18 Using a Schottky diode and capacitor to supply local power on the 1-Wire net.

Transfer charge to a capacitor through a blocking diode

For some applications it may be acceptable to use a series Schottky diode and capacitor across the 1-Wire bus to generate a local supply on the net at the point of interest. Refer to **Figure 18**. The wind speed sensor in the 1-Wire weather station which uses a BAT54S for the Schottky diode and a .01μF ceramic capacitor to power the DS2423 counter uses this technique. See **Figure 23**. During idle communication periods when the bus is at 5V, the circuit 'steals' power from the line to charge the capacitor and power the load. This is a discrete implementation of the parasite power technique used internally by 1-Wire devices to provide their own operating power. The value used for C1 depends on the current consumption of its load and how long the voltage must be held above a design value. While simple and economical the circuit adds both leakage and capacitive loads that reduce the range and capability of the 1-Wire net. This loading places an upper limit on the capacitance value used and the number that can be placed on the net. Consideration must also be given to the fact that in the event the capacitor is shorted or held in a discharged state by its load, the net will also be shorted and inoperable. No further communication can take place until the capacitor is charged above 3.5 volts.

Deliver energy under bus master control

As shown in **Figure 19**, the half wave rectifier of **Figure 18** can be isolated between two addressable switches controlled by the master. When the input switch is closed, the capacitor receives charge over the DATA line of the 1-Wire net in the same manner as the circuit of **Figure 18**. A significant advantage of the arrangement is that when the switch is opened the capacitor and its charge is isolated from the net and normal communication resumes without the burden of the capacitive and leakage loads of C1. When the stored energy is needed, the output (power dump) switch is closed and the capacitor is discharged through the load. Note that while reference was made to a capacitor, a rechargeable battery could be used equally as well. Important elements of the concept and architecture are the low-level transfer of energy from the bus master to a storage element, and subsequent use in a high energy burst. Conceptionally, this is somewhat similar to the way circuitry in a flash camera develops the energy needed to fire a flashbulb. Equally important is the isolation of the storage element from the 1-Wire net so a failure doesn't bring down the net, and the complete control of energy source delivery by the bus master.

A practical example of the concept using a DS2406 as the control element and pFETs for the switches is shown in **Figure 20**. Notice that the MICREL MIC94031 FET isolation switches specified are four terminal devices with the substrate terminal brought out. This provides for correct biasing of the terminal under all operating conditions. The gate pull-up resistor shown unlabeled is internal to the chip but shown for clarity. In order to insure that both switches can not be turned on at the same time and

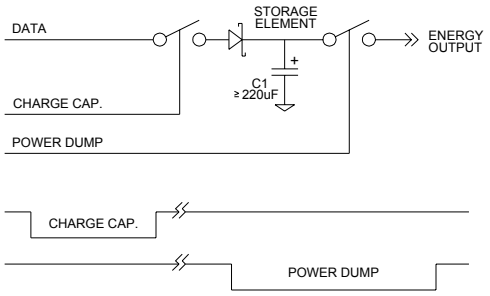

Figure 19 A parasite powered 1-Wire remote high-energy source concept.

possibly bring down the net, a lockout circuit is constructed using U2, a 74HC126 tri-state gate. By design U2 only allows alternate enabling of the pass gates to charge and discharge the energy storage element C1. As shown in the truth table of **Figure 20**, if both outputs of the DS2406 are simultaneously placed in the same logic state, either intentionally or by accident, U2 insures that neither pass gate is turned on.

In operation, C1 is charged by commanding output B of U1 (pin 6) the DS2406 to a logic zero. This turns on Q1, connecting the 1-Wire DATA line to C1 through diode CR2 which prevents C1 from discharging back through the 1-Wire net. If the diode were not present and a 1-Wire device were to be placed on the bus when the pass gate was turned on, its Presence Pulse would short and discharge the capacitor possibly damaging the chip. In the initial state with no charge on C1, the gate of Q2 the discharge pass gate, is held at a higher potential then the source terminal by pull-up resistor R4, so Q2 is off. When the bus master turns output B of U1 off, the charge stored on C1 is isolated from both the 1-Wire net and the load and only leakage paths exist to discharge it. When the bus master commands output A of U1 (pin 3) to a logic zero, pass gate Q2 turns on and C1 discharges through the load.

In a more sophisticated implementation of the concept, a barometric sensor was constructed using U1, a DS2450 Quad ADC as the 1-Wire addressable switch control element. The DS2450 also reads the charge level of the energy storage capacitor C1 and controls a sample-and-hold on the output of the

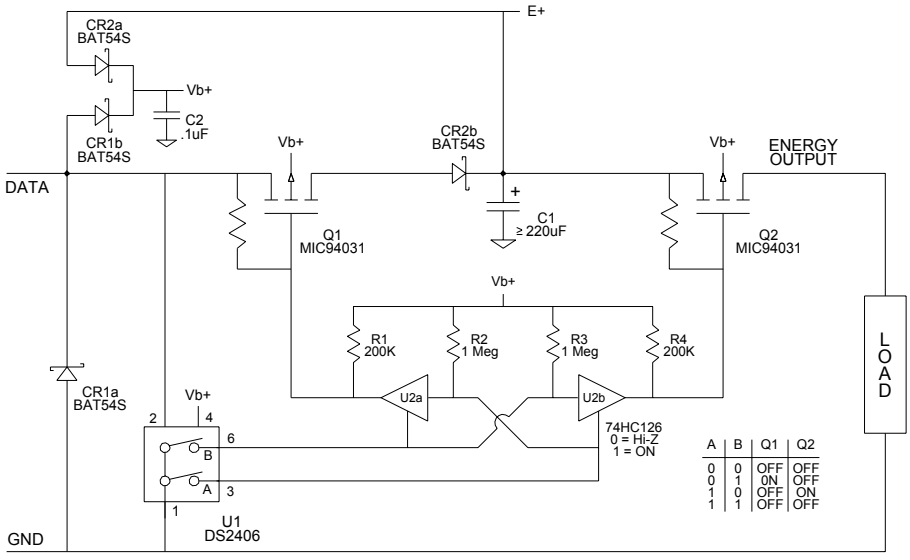

Figure 20 An isolated remote energy source based on the DS2406 addressable switch.

sensor. A major design consideration of the circuit was that the barometer required the energy source C1 to provide up to 10mA for 22mS. A schematic of the prototype circuit is shown in **Figure 21**. In the circuit, two DS2450 I/O pins are used as digital outputs that control the capacitor charge and discharge via analog switch U3 and a specialized switched-capacitor voltage regulator U4 used in place of the output (discharge) analog switch. The charge pump, a MAX684 from MAXIM, provides a regulated 5V ± 4% output as the energy capacitor discharges down to 2.7V. Surprisingly, the efficiency increases as the input voltage drops, a very useful feature when using a discharging capacitor as the energy source. The two remaining I/O pins of U1 are used as analog inputs which read the voltage on storage capacitor C1, and the voltage from the sample-and-hold (U7) that stores the output from the barometer representing the current barometric pressure. The circuit performed as expected with values up to 0.22 Farad for C1 the energy storage capacitor. Obviously, the higher the capacitance, the longer it takes to charge and the longer the voltage level is maintained relatively constant.

In operation, pulling U1.7 low closes analog switch U3 allowing C1 to charge through CR1. CR1 prevents C1 from discharging back through the 1-Wire net. The voltage generated by charging C1 can be read as needed by U1.8 to insure that sufficient energy exists to operate the load. When U1.7 is turned off, analog switch U3 also turns off and the charge stored on C1 is completely isolated from the net. At the appropriate time, U1.6 is pulled low which enables voltage regulator U4 providing a path for C1 to discharge through barometer U5. The MPXA4115 Motorola part requires 22mS maximum to turn on and stabilize, at the end of which time the output voltage representing current atmospheric pressure is stored on C3 the sampling capacitor. After the sample, U4 turns off to minimize energy loss from the storage capacitor C1. Instead of the wide interval used in the prototype circuit to sample the barometer it would be preferable to use a narrow pulse immediately after the output has settled.

Use additional available wires

In order to obtain maximum performance, Dallas Semiconductor recommends CAT 5 UTP (unshielded twisted pair) for use in routing the 1-Wire net. However, since CAT 5 typically comes with multiple pairs, there is a natural inclination to use an extra pair to route power. A look at some cable properties will help in understanding how such an arrangement affects net performance. In a CAT 5 cable with multiple twisted pairs, on average any given conductor in

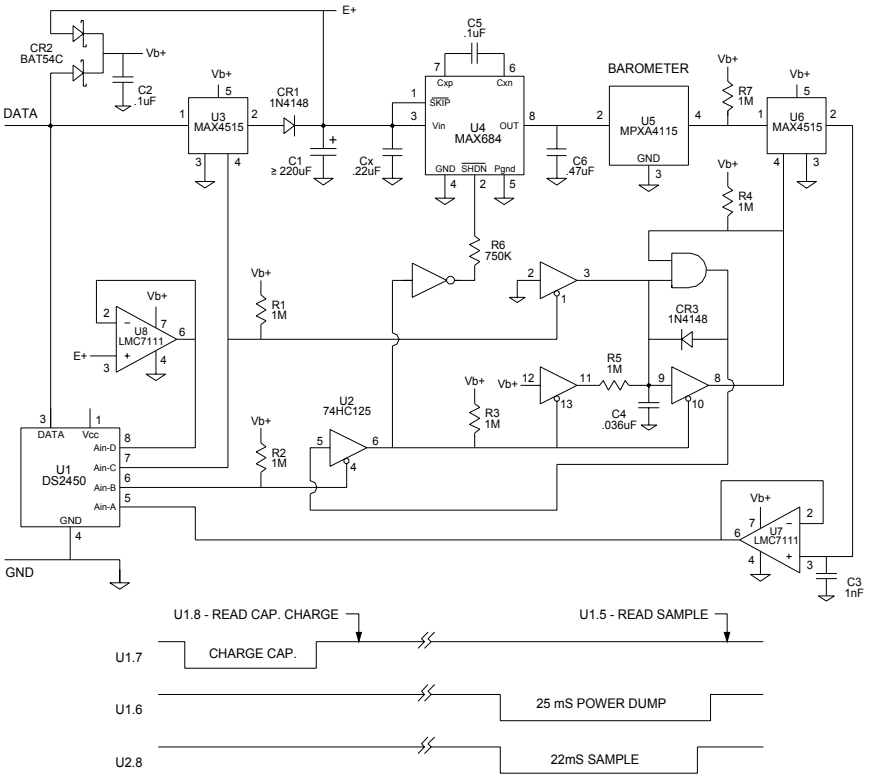

Figure 21 A 1-Wire barometer powered off the bus by an isolated and regulated energy source.

a pair is adjacent to a second conductor in another pair for half its length. Typically, the capacitance between the two conductors of a twisted pair is approximately 50 pF/m while that between the conductors of two different pair runs about 30 pF/m. Because grounding unused conductors will increase the capacitive load seen by the master, Dallas Semiconductor recommends that unused wires and shields be left unconnected at both ends of the cable. Still, within the limits set by increased capacitive loading and potential cross talk caused by using the extra pairs within the cable, external power can be routed along with the 1-Wire DATA and GND pair. However, the loading can reduce how long the bus can be and/or the number of 1-Wire devices the net can support. In addition, current and voltage variations on the pair carrying power can induce cross talk on the 1-Wire DATA and GND that disrupts communication.

Since the bus master sees less capacitive loading when routing power over flat cable where the conductors maintain a fixed and distant separation, flat 6-conductor phone (silver satin) may be used up to about 200 feet. Insure that DATA and GND have maximum separation from the power conductors by using the outer two conductors next to the 1-Wire GND to carry power. As shown in **Figure 22**, the wiring sequence should proceed in this order; NC (no connection); NC; 1-Wire DATA; 1-Wire GND, then external power and ground on the two outermost conductors. This arrangement helps shield the critical DATA lead from the additional capacitive load and cross talk of the external power leads. Notice again that the two conductors prior to the 1-Wire DATA line shown in dashed lines are to be left uncommitted. As repeatedly emphasized, if connected they will substantially increase the capacitive load seen by the DATA line. One possibility is to use 4-conductor silver satin and assemble the cable with

these two slots in the RJ11 connector empty. Unfortunately, a significant disadvantage of flat cable is that it lacks the noise rejection properties of twisted pair cable, so EMI may present a significant performance problem if the net is routed near sources of electrical noise.

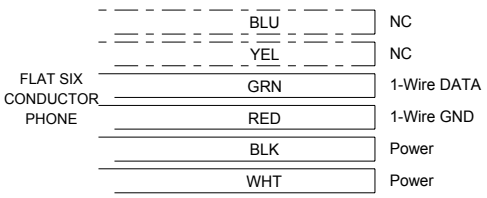

Figure 22 If power is to be routed over flat phone wire along with 1-Wire DATA and GND, use the outer two conductors by 1-Wire GND to minimize cross-talk and capacitive loading.

CHAPTER 4
1-Wire Instrumentation

In addition to 1-Wire control chips such as the DS2406 and DS2409, several digital functions such as temperature sensors and analog-to-digital (ADCs) converters are available. These make it possible to measure a wide variety of physical properties over the 1-Wire net. A distinct advantage of 1-Wire instruments is that all interface to the master in the same manner regardless of the particular property being measuring. Whether the basic sensing element is voltage, current, resistive or capacitive based, they all communicate over the net using 1-Wire protocol. Other methods employ a variety of signal conditioning circuitry such as instrumentation amplifiers and voltage-to-frequency converters which of necessity makes their outputs different and may require separate cables for each sensor. The unique ID address or serial number of each device is the key for the bus master to interpret what parameter a particular 1-Wire instrument is measuring. Since the science of meteorology requires a variety of diverse sensors, several examples of 1-Wire instrumentation for use in a weather station will be given here. For example, the DS2423 Counter has inputs which respond to logic level changes or switch closures making them suitable to implement a variety of rate sensors. An example using magnetically actuated reed switches suitable for a rain gauge or wind speed sensor is shown in **Figure 23**.

Counting with the DS2423 1-Wire Counter

In the figure, the dual diode BAT54S serves both to protect the circuit from signals that go below ground, and with C1, to provide a local source of power. While the DS2423 has an internal pull-up resistor to keep the input from floating, its high value (≈ 22 Meg Ohms) can make it susceptible to noise. To prevent generating spurious counts during turn-on, and minimize noise pick-up, an external 1 Meg Ohm pull down resistor is used instead. Except for Lithium back-up (not shown), this is the counter circuit used in the 1-Wire rain gauge. In that application, a small permanent magnet moves past the reed switch each time a tipping bucket fills and empties. This momentarily closes the reed switch which increments the counter indicating .01 inch of rain has fallen.[1] A similar circuit is used in the 1-Wire weather station to measure wind speed.[2] The same circuit with Lithium backup has also been used as a hub mounted wheel odometer. Conveniently, the DS2423 also contains 4096 bits of user accessible SRAM, which is useful for temporary storage, or with Lithium back-up, for calibration, location and function information.

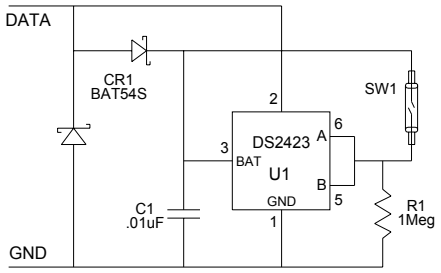

Figure 23 The basic DS2423 Counter circuit.

The DS2438, a versatile performer

Originally designed to perform multiple functions in a battery pack, the DS2438 contains two ADCs and a temperature sensor. The main ADC performs 10-bit conversion on a 0-10V input, or 9-bit conversion on a 0-5V signal, with an internal multiplexer that allows it to read the voltage on its power supply pin. The other converter was intended to measure the voltage developed by large currents flowing across an external .05 Ohm resistor with 10-bit accuracy at a full-scale reading of ± 250mV. The 13-bit internal temperature sensor is similar to the DS18B20. Additional features include a Real Time Clock and 40-bytes of nonvolatile memory useful for storing calibration, location and function information.

Measuring Humidity over the 1-Wire

Humidity is an important factor in many manufacturing operations as well as affecting personal comfort. With the proper sensing element, it can be measured over the 1-Wire net. The Honeywell sensing element specified here develops a linear voltage versus relative humidity (RH) output that is ratiometric to supply

voltage. That is, when the supply voltage varies, the sensor output voltage follows in direct proportion. This requires that the voltage across the sensor element as well as its output voltage be measured. In addition, calculation of True RH requires knowledge of the temperature at the sensing element. Because it contains all the necessary measurement functions to do the calculations, the DS2438 makes an ideal choice to construct a humidity sensor.

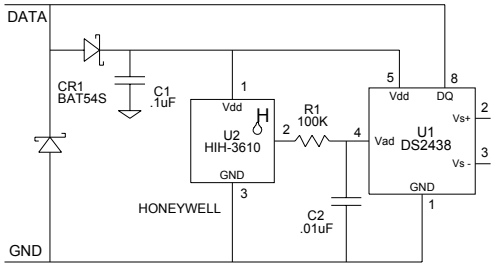

Figure 24 A humidity sensor using the DS2438.

In **Figure 24**, the analog output of the HIH-3610 humidity sensing element is converted to digital by the main ADC input of a DS2438. As in the DS2423 Counter circuit, a dual-diode BAT54S serves both to protect the circuit from signals that go below ground, and with C1, to provide a local source of power. Notice that C1 has been increased from .01uF to .1uF to handle the operating current required by U2, the HIH-3610. The RC network on the output of U2 is a low pass filter used to remove the low level clock feed-through from the sensing element's signal conditioning circuitry. However, if averaging is done in software, R1 and C2 are not necessay and may be omitted.

In operation, the bus master first has U1, the DS2438, report the supply voltage level on its Vdd pin, which is also the supply voltage for U2, the sensing element. Next, the master has U1 read the output voltage of U2 and report local temperature from its on-chip sensor. Finally, the master calculates true relative humidity from the three parameters supplied by U1.[3]

A 1-Wire Barometer Using the DS2438

Barometric pressure is another important meteorological parameter that can be measured over a 1-Wire net using the DS2438. By selecting a pressure sensor that contains comprehensive on-chip signal conditioning circuitry the circuit in **Figure 25** is very straightforward. As was the case with the humidity sensing element, the specified pressure sensing element is ratiometric. This requires that both the output voltage representing atmospheric pressure and the supply voltage across the element be known in order to accurately calculate barometric pressure.

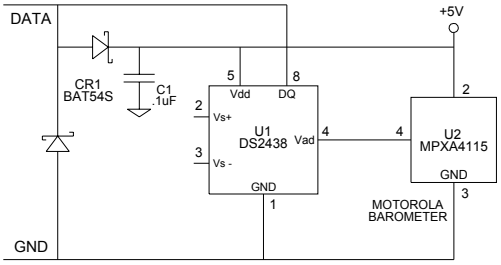

Figure 25 The 1-Wire barometric pressure sensor.

As is typical for 1-Wire instrumentation, a dual-diode BAT54S serves to protect the circuitry from signals that go below ground, and with C1, to provide a local source of power. In this case, because U2, the MPXA4115 pressure sensor can require as much as 10 mA at 5V, an external source of power is needed. Notice that the external power is also connected to the power pin of the DS2438. This allows the DS2438 to measure the supply voltage applied to the pressure sensing element. Alternatively, the barometer can be powered directly off the 1-Wire net by using concepts described in **Chapter 3**. However, in many installations supplying external power is not a problem as the barometer will be mounted inside near the bus master and a source of power. Flexible tubing can be routed to sample the outside air pressure and avoid unwanted pressure changes (noise) caused by the opening and closing of doors and windows or elevators moving inside the building.

A Wind Direction Sensor Using the DS2450

While the original 1-Wire weather station used a DS2401 Silicon Serial Number to label each of the eight magnetic reed switches in its wind direction sensor, a single D2450 Quad ADC can perform the same functions.[2] In keeping with recommendations for an ADI, a dual-diode BAT54S serves to protect the circuitry from signals that go below ground, and with C1, to provide a local source of power. Note that C1 has been increased from .01uF to 10uF to insure that the voltage across the resistor network remains relatively constant. As shown in **Figure 26**, a single DS2450 replaces the eight DS2401s originally used with five resistors. As the wind rotates the wind vane, a magnet mounted on a rotor that tracks it opens and closes one (or two) of the reed switches. When a reed switch closes, it changes the voltages seen on

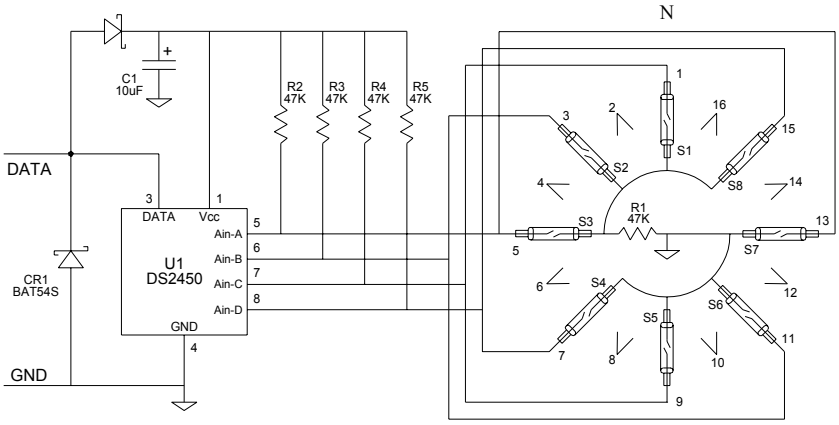

Figure 26 A wind direction sensor using the DS2450 Quad ADC.

the input pins of U1, the DS2450. For example, if the magnet is in a position to close S1 (North), the voltage seen on pin 7 changes from Vcc to 1/2Vcc, or approximately, from 5V to 2.5V. Since all sixteen positions of the wind vane produce unique four-bit signals from the ADC, there is no need to initialize the sensor, or store a tagging code on the board as was required by the original 1-Wire weather station. It is only necessary to indicate North, or equivalently, which direction the wind vane is pointing. **Table 1** lists the voltages seem at the ADC inputs for all sixteen cardinal points.

POS.	D	C	B	A
1	5	2.5	5	5
2	5	3.3	3.3	5
3	5	5	2.5	5
4	5	5	3.3	3.3
5	5	5	5	2.5
6	0	5	5	2.5
7	0	5	5	5
8	0	0	5	5
9	5	0	5	5
10	5	0	0	5
11	5	5	0	5
12	5	5	0	0
13	5	5	5	0
14	2.5	5	5	0
15	2.5	5	5	5
16	3.3	3.3	5	5

Table 1 Wind vane position versus voltage seen at the four DS2450 ADC inputs.

Because two reed switches are closed when the magnet is midway between them sixteen compass points are indicated with just eight reed switches. Referring to the schematic and position 2 in **Table 1**, observe that when S1 and S2 are closed 3.3 Volts is

applied to ADC inputs A and B. This occurs because pull-up resistors R2 and R3 are placed in parallel and the pair connected in series with R1 to form a voltage divider with .66Vcc across R1. Notice that this also occurs twice more at switch positions 4 and 16.

Measuring Solar Radiance on the 1-Wire

The amount of sunlight and its duration are additional parameters that meteorologists are interested in measuring. The ***amount*** is a measure of air and sky conditions, while ***duration*** is related to the equinoxes and the length of the day. While mounting and filtering tend to be complex, as shown in the following two figures, the electronics can be easily implemented using the DS2438. **Figure 27** illustrates a Solar radiance sensor using a photodiode, while **Figure 28** uses a photovoltaic cell. In each case a dual-diode BAT54S serves to protect the circuitry from signals that go below ground, and with C1, to provide a local source of power.

In **Figure 27** a sense resistor is connected in series with a photodiode and between the two 'current' ADC pins. Light striking the photodiode generates photo

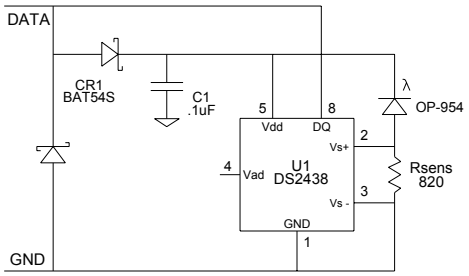

Figure 27 A Photodiode Solar radiance sensor.

currents that in turn develop a voltage drop across the sense resistor that is read by the ADC. In commercial units, optical filters are added to control both the wavelength and bandpass to which the sensor responds. More sophisticated units add such desirable features as a translucent hemisphere that collects light to enable the sensor to view the sky from horizon to horizon. In this case, the sensor actually focuses on the inside of the hemisphere to obtain its reading.

An interesting variation of a solar radiance sensor can be constructed using an LED in reverse bias mode. Select an LED that has acceptable current levels when exposed to the sun at high noon on a clear day. Size the resistor to develop 250 millivolts maximum using the formula R = E divided by I where E is 0.25 Volts and I is the maximum current generated. One example is the EFA5364X from Stanley. This is a super-bright orange ALGaInP LED with a peak response at 609nm and a narrow 15° spectral field of view. A 4.7K sense resistor provides acceptable outdoor performance, which may be increased to 100K if the circuit is only to be used with indoor lighting. LEDs made from other compounds will have their peak response in a different portion of the spectrum making them useful in specific applications.

Another approach to a solar radiance sensor is shown in **Figure 28** where a suitable solar cell is connected to the 'current' ADC inputs of the DS2438 through voltage divider R1 and R2. The divider is necessary to ensure that the voltage between pins 2 and 3 of the DS2438 does not exceed its maximum limit of 300 millivolts. Chose resistor values for the divider so as to not unduly load the power capacity of the cell. C2 and R3 form a low-pass filter to reduce noise sensitivity. One advantage of this technique is the ability to use several cells facing toward different

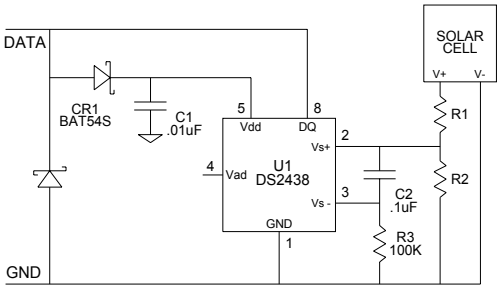

Figure 28 A Solar radiance sensor using a photovoltaic cell.

sectors of the sky to obtain horizon to horizon coverage. Connect the cells in parallel and size R2 to develop 0.25 Volts with maximum sun light across the sensor as described in the preceding paragraph.

MEASURING A THERMOCOUPLE WITH 1-WIRE

It is also posssible to measure extreme temperatures using conventional thermocouples that are directly digitized at the cold junction using a DS2760 multi-

function 1-Wire chip. The twisted pair cable of the 1-Wire net serves to cover the distance between the (TC) and bus master effectively replacing the expensive thermocouple (TC) extension cable normally used. Because of its unique ID address multiple smart thermocouples may be placed where needed anywhere along the net greatly minimizing the positioning and cost of an installation. Although information associated with the TC may be stored within the chip itself ("tagging"), this same ID allows reference data to be stored at the bus master. [4]

REVIEWING THE THERMOCOUPLE

The fundamental operating principle of the thermocouple was discovered in 1821, when Thomas Seebeck discovered that if two dissimilar metals were joined at one end a voltage (the Seebeck Voltage) proportional to the temperature difference between the joined and open ends was generated. Two of the more popular industry standards are the type K and type E. By convention capital letters are used to indicate composition according to American National Standards Institute (ANSI) conventions. For example, type E thermocouples use nickel-chromium as one conductor and constantan (a copper-nickel alloy) as the other. While the full-scale output voltage of all TCs falls in the low millivolt range, the type E generates the highest Seebeck Voltage/°C (62μV/°C @20°C) resulting in an output of almost 80 millivolts at 900°C; more than any other standard. Obviously, in order to measure this output voltage it is necessary to make connections to the open ends of the wires forming the thermocouple. These connections in turn form a second thermocouple, for example nickel-chromium/copper in series with the original or 'hot' junction when copper conductors are used. Historically to correct for these 'cold' junctions (one for each TC wire) they were placed in an ice bath at the triple point, whereas most modern instruments electronically correct the reading to zero degrees.

When electronic correction is used, the temperature at the cold junction is measured and the voltage that would be generated by the thermocouple at that temperature is subtracted from the actual reading. If the voltage versus temperature transfer function of the thermocouple were highly linear this would be all that was necessary to correct the reading. Unfortunately, since the Seebeck Voltage /°C varies with temperature, the full-scale transfer function is usually fairly complex which can require several piece-wise approximations to maintain a specified accuracy depending upon the temperature range of interest. In this respect, the type K TC with its lower Seebeck Voltage (51μV/°C @20°C) has an advantage over the type E as it is significantly more linear over the 0°C to 1000°C range. For in-depth information on thermocouples, check the reference material available on the web by manufacturers such as Omega Engineering Inc.[5]

While there are obvious variations, a typical modern electronic thermocouple consists of several basic building blocks. As illustrated in **Figure 29**, these blocks consist of a TC with secondary temperature sensor to measure the junction where thermocouple and connecting wires join; a signal conditioning block and an analog-to-digital converter (ADC). Usually, the thermocouple is connected to a precision low noise or instrumentation amplifier, which provides the gain, offset and impedance adjustments necessary to match the low level signal generated by the TC to the input of a multi-bit ADC. The ADC in turn converts the conditioned signal from the amplifier into a digital format that is sent to a microprocessor or PC. From the ADC and cold junction sensor inputs, the μP (or PC) computes the actual temperature seen at the hot junction of the thermocouple. Some custom conditioning chips such as the MAX6675 from Maxim or the AD594 from Analog Devices are available that contain both the instrumentation amplifier and the cold junction compensation circuitry for a particular TC type such as the J or K in one IC. These chips replace the first two blocks and plug directly into an ADC input.

THE DS2760

Originally designed to monitor a Lithium-Ion battery pack, the DS2760 provides several new capabilities to transform a simple thermocouple into a smart sensor.[6] The chip can directly digitize the millivolt level output produced between the hot and cold junctions of the thermocouple, while it's on-chip temperature sensor continuously monitors the temperature at the cold junction of the TC. With its unique ID address it provides a label that permits

multiple units to operate on the same twisted pair cable. And it contains user accessible memory for

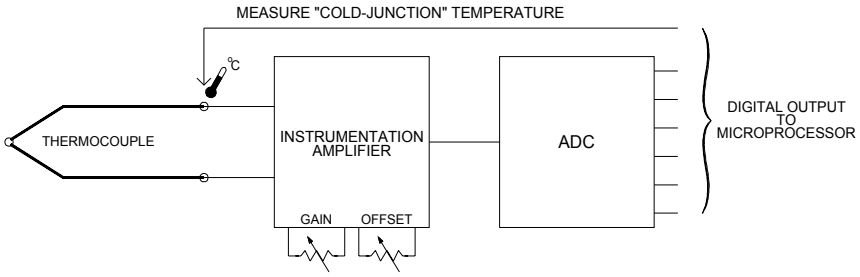

Figure 29 A typical electronically compensated thermocouple consists of these three building blocks.

storage of sensor specific data such as TC type, location and the date it was placed into service. This allows a DS2760 to be used with any TC type as the bus master uses the stored data to determine the correct calculations to make based on the type TC in use and the temperature of the cold junction as reported by the on-chip temperature sensor.

As a complete signal conditioning and digitizing solution for use with a thermocouple, the DS2760 contains a 10-bit voltage ADC input, a 13-bit temperature ADC and a 12-bit plus sign current ADC. It also provides 32-byte of lockable EEPROM memory where pertinent user or sensor documentation may be stored which can minimize the probability of error due to the mislabeling of sensors. In the present application, the thermocouple is directly connected to the current ADC inputs that were originally designed to read the voltage drop developed across a 25 milli-Ohm resistor as a Lithium-Ion battery pack is charged and discharged. With a full scale range of ± 64 millivolts (LSB of 15.625μV) the converter provides resolution exceeding one degree C even with the lower output of a Type K thermocouple.

THE 1-WIRE THERMOCOUPLE

The schematic in **Figure 30** illustrates both the simplicity and ease with which a DS2760 can be used to convert a standard thermocouple into a smart sensor with multi-drop capability. In the circuit, C1 and one of the Schottky diodes in CR1 form a half wave rectifier that provides power for the DS2760 by 'stealing' it from the bus during idle communication periods when the bus is at 5V. This is a discrete implementation of the parasite power technique used internally by 1-Wire devices to provide their own operating power. The remaining Schottky diode in the package is connected across DATA and GND and provides circuit protection by restricting signal excursions that go below ground to about minus four tenths of a volt. Without this diode, negative signal excursions on the bus in excess of six tenths of a volt forward bias the parasitic substrate diode of the DS2760 chip and interfere with the proper functioning of the chip. Under bus master control U1 the DS2760, monitors the voltage developed between the hot and cold junctions of the thermocouple as well as measuring the temperature of the cold junction with its internal temperature sensor. The master uses this information to calculate the actual temperature at the hot junction of the TC. By adding the optional resistor (R1), Vdd may also be measured. This can be useful in trouble-shooting to verify that the voltage available on the 1-Wire net is within acceptable limits.

When mounting the thermocouple to the board, it should be connected as close to the DS2760 as practical so minimal temperature difference exists between these connections and the chip inside the DS2760 package. To maintain the junctions at the same temperature use copper pour and lead placement to create an isothermal area in and around the point where the thermocouple leads attach to the copper traces of the PCB. Keeping in mind that temperature differentials generate voltage differentials over their entire length, route the PCB

traces together and maintain equal numbers of junctions on each conductor.

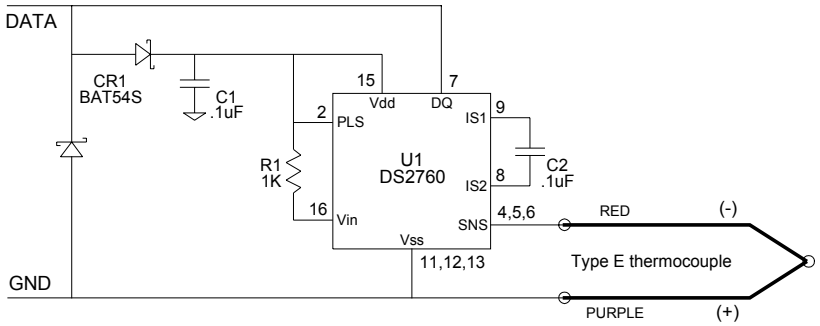

Figure 30 Using a DS2760 to read a thermocouple on the 1-Wire net.

1-Wire®, TMEX AND 1-Wire net are trademarks of Dallas Semiconductor.

REFERENCE

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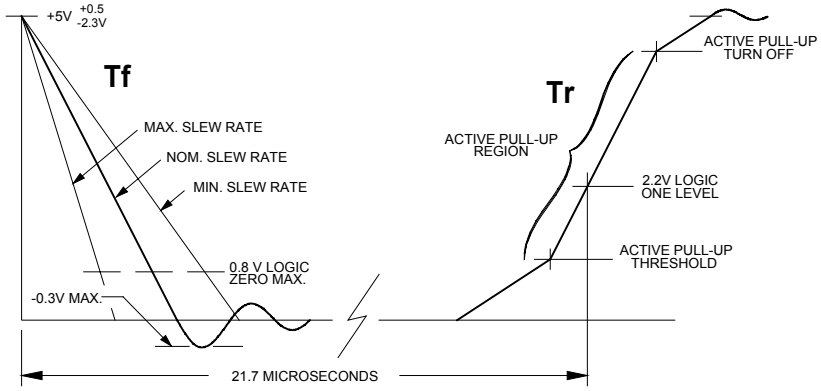
6. DS2760 data sheet. http://pdfserv.maxim-ic.com/arpdf/DS2760.pdf.

APPENDIX A
Waveform template for a 1-Wire net exceeding 100 meters



This section defines the 1-Wire template for use with bus lengths exceeding 100 meters. Notice that the zero to one transition is shown with the characteristic waveform for an active pull-up as the use of a passive pull-up resistor can be problematic with cables of this length. A 5V pull-up supply is recommended, but can range from 3 to 6 volts.

The falling edge (Tf)

Because it controls all system timing, the falling edge of the waveform from the bus master should be monotonic. To prevent signal disruptions caused by unterminated transmission line effects, the slew rate must be controlled to be much longer than twice the electrical length of the cable. This works out to be about 1.1volts per microsecond (V/µS) for the given conditions. As shown in the template, this requires 4 microseconds to cross the 0.8V logic zero threshold level. This slew rate provides acceptable performance with bus lengths up to 300 meters. It performs well over that range with 1-Wire loading varying from one to 500 devices.

For net communication to be successful, the bus must be raised to a voltage greater than the 2.2V logic one level before the master samples. Beginning with TMEX v3.0, sampling occurs 21.7µS after the master pulls the bus low. If the bus pull-up fails to raise the voltage above the logic one threshold before this sampling occurs, the master will always see a logic zero and conclude the bus is shorted, and communication can not occur.

Negative Undershoot

Signal excursions below ground must be clamped to less than 0.6V to prevent turning on parasitic diodes in the substrate.

The rising edge (Tr)

As the number of 1-Wire devices on the bus grows, the time required to raise the line above the logic one threshold increases. This also occurs as the network is lengthened due to the 50pF of capacitance added per meter of twisted pair cable. Because of these effects, for a 1-Wire net of 100 meters or more, an active pull-up must be used. Obviously, an active pull-up circuit should be on only during a defined range of the rising edge (zero to one transition). Conversely, it should not respond on the falling edge, nor be active during logic zero time intervals. It must trigger on the rising edge at about 0.9V plus or minus 0.1V to provide acceptable noise margin. Preferably, once triggered it will remain on until the line is raised above a specified threshold (≥3V) rather than for a set time interval (one-shot). This insures that the data line will be raised above the 2.8V level required to recharge the parasite power capacitors regardless of load. The maximum current the circuit can supply should be limited to about

15mA. Larger currents flowing in cable inductance can cause problems.

Consult the Dallas Semiconductor iButton website at **www.ibutton.com** for current product information, application notes and data sheets.