MQ222-02

EPSON

Application Manual

Real Time Clock Module

RTC-4513

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SEIKO EPSON CORPORATION

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CONTENTS

Serial Interface Real Time Clock Module

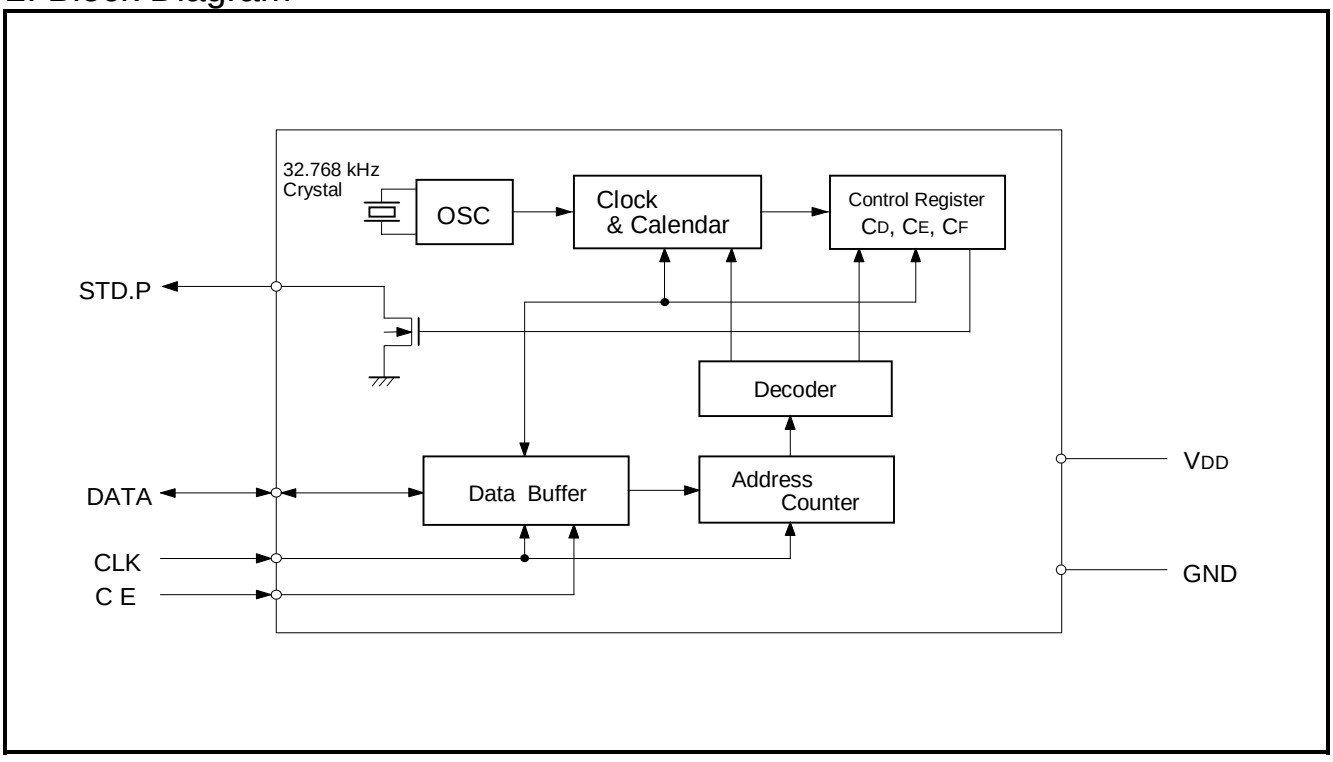
RTC - 4513

- Built-in frequency adjusted 32.768 kHz quartz crystal
- Serial interface controllable by three signal lines
- Four types of fixed-period interrupts (or waveform output)
- Automatic leap year compensation
- Software 30-second adjustment function
- Wide operating voltage range (2.7 V to 5.5 V)
- Wide data preservation range (2.0 V to 5.5 V)
- Low current consumption
- Compact SOP-14 package ideal for high integration applications

1. Overview

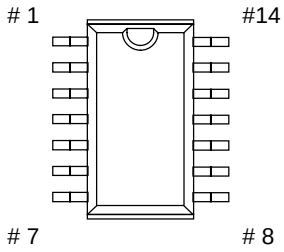
The RTC-4513 is a serial interface real time clock with integrated quartz oscillator. It provides a wide array of features, including clock and calendar functions, as well as fixed-period interrupts, 30-second adjustment, automatic leap year compensation, and oscillation stop detection. The serial interface can be controlled by three signal lines, to keep the number of ports on the system side to a minimum. The SOP-14 package is well suited for highly integrated installations where space is at a premium, such as in portable phones, handheld terminals and many other compact electronic devices.

2. Block Diagram



3. Pin Assignment

RTC - 4513



SOP - 14 pin

4. Pin Functions

Signal	Pin no.	I/O	Function
DATA	2	Bi-directional	This pin serves for write mode/read mode selection, address write, and data read/write operations. Becomes either a high-impedance input pin or an output pin, depending on the write mode/read mode setting in the first 8 bits of the input data after the rising edge of the CE input.
STD.P	3	Output	This pin operates as fixed-cycle open-drain output for the N channel, or as interrupt output for the CPU. The fixed-cycle output serves for verification of the reference signal or the oscillation frequency. Selection of fixed-cycle or interrupt output is performed by writing the INT/STND bit. This output is not disabled by the CE pin. (For details, refer to the section entitled "Description of Registers.")
V_{DD}	6		Connect to the positive side of the power supply. The voltage must be 2.7 to 5.5 V during normal operation and at least 2.0 V during battery backup operation.
GND	9		Connect to the negative (grounded) side of the power supply.
C E	12	Input	Chip enable input pin. When high, the chip is enabled. When low, the DATA pin goes to high impedance, the DATA pin and CLK pin are disabled within the LSI, and the feed through current is cut off. Furthermore, setting the CE pin low forcibly clears the fr, TEST, and RESET bits to "0". Note that this pin should be low when the power supply is turned on.
CLK	13	Input	Shift clock input. At the rising edge of this signal, data are read (write mode) or output (read mode).
N.C.	1,4,5,7,8, 10,11,14	—	These pins are internally not connected, but to assure stable oscillation, connect them to V_{DD} externally.

* Be sure to connect a bypass capacitor of at least 0.1 μF between V_{DD} and GND.

5. Specifications

5-1. Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta=+25 °C	–0.3 to 7.0	V
Input voltage	V_I		GND–0.3 to V_{DD}+0.3	
Output voltage	V_O		GND–0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	–	–55 to +125	°C
Soldering conditions	TSOL	Max. 2 times under 10 seconds below a temperature of +260 °C or for 3 minutes below a temperature of +230 °C		

5-2. Operating conditions

Item	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	–	2.7 to 5.5	V
Clock power supply voltage	V_{CLK}	–	2.0 to 5.5	V
Operating temperature	T_{OPR}	No condensation	–40 to +85	°C

5-3. Oscillation characteristics

Item	Symbol	Condition	Rating	Unit
Frequency tolerance	Δf/fo	Ta=+25 °C , V_{DD}=3.0 V	0 ± 25	$\times 10^{-6}$
Frequency Temperature characteristics	Top	–10 to +70 °C , +25 °C Standard	+10 / –120	$\times 10^{-6}$
Frequency voltage characteristics	f/V	Ta=+25 °C , V_{DD}=2.0 to 5.5 V	± 5 (Typ.)	$\times 10^{-6}$ / V
Oscillation start time	tSTA	Ta=+25 °C , VDD=3.0V	3 (Max)	s
Aging	fa	Ta=+25 °C , VDD=3.0V *1	± 5	$\times 10^{-6}$ / year

*1) At starting year

5-4. DC characteristics

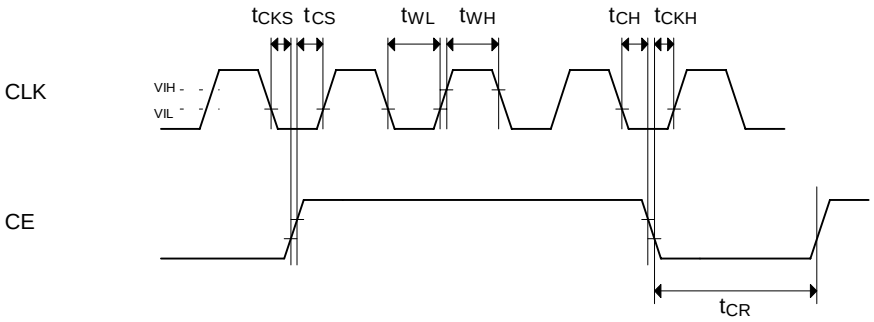
∗ GND=0 V , V_{DD}=2.7 V to 5.5 V , Ta= –40 to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pins
High input voltage	V_{IH}	–	0.8V_{DD}	–	–	V	Input pins
Low input voltage	V_{IL}	–	–	–	0.2V_{DD}	V	Input pins
Input leakage current (1)	I_{LK1}	V_I=V_{DD}/GND	–	–	1 / –1	µA	CE,CLK
Input leakage current (2)	I_{LK2}	V_I=V_{DD}/GND	–	–	10 / –10	µA	DATA
Low output voltage (1)	V_{OL1}	Io=1 mA	–	–	0.2V_{DD}	V	DATA
High output voltage	V_{OH}	Io= –400 µA	0.8V_{DD}	–	–	V	DATA
Low output voltage (2)	V_{OL2}	Io=1 mA	–	–	0.2V_{DD}	V	STD.P
OFF leakage current	I_{OFLK}	Vo=V_{DD}	–	–	10	µA	STD.P
Current consumption (1)	I_{DD1}	V_{DD}=5 V,V_I(CE)=0 V	–	10	20	µA	V_{DD}
Current consumption (2)	I_{DD2}	V_{DD}=3 V,V_I(CE)=0 V	–	2.5	5.0	µA	V_{DD}
Current consumption (3)	I_{DD3}	V_{DD}=2 V,V_I(CE)=0 V	–	1.0	2.0	µA	V_{DD}

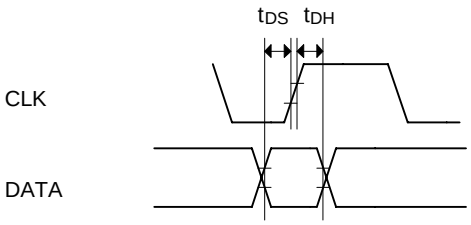
5-5. AC characteristics

∗ GND=0V , V_{DD}=2.7 V to 5.5 V , Ta= −40 to +85 °C

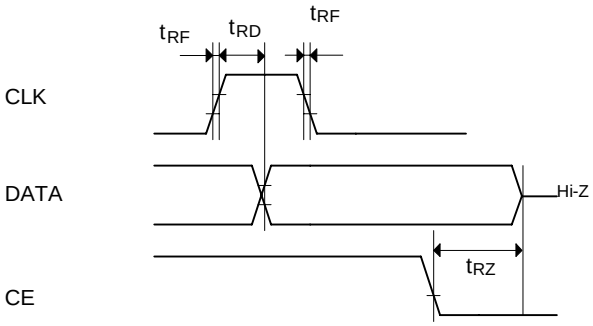
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK H pulse width	t_{WH}	–	300	–	–	ns
CLK L pulse width	t_{WL}	–	300	–	–	ns
CE setup time	t_{CS}	–	150	–	–	ns
CE hold time	t_{CH}	–	200	–	–	ns
CE recovery time	t_{CR}	–	300	–	–	ns
CLK setup time	t_{CKS}	–	20	–	–	ns
CLK hold time	t_{CKH}	–	20	–	–	ns
Write data setup time	t_{DS}	–	50	–	–	ns
Write data hold time	t_{DH}	–	50	–	–	ns
Read data delay time	t_{RD}	CL=50 pF	–	–	250	ns
Output disable delay time	t_{RZ}	–	–	–	100	ns
Input rise time/fall time	t_{RF}	–	–	–	20	ns



WRITE MODE



READ MODE



6. Registers

6-1. Register Table

Address	Register name	D3 (MSB)	D2	D1	D0 (LSB)	Count range	Remarks
0	S_1	s8	s4	s2	s1	0~9	1-second digit register
1	S_{10}	fo	s40	s20	s10	0~5	10-second digit register
2	MI_1	mi8	mi4	mi2	mi1	0~9	1-minute digit register
3	MI_{10}	fr	mi40	mi20	mi10	0~5	10-minute digit register
4	H_1	h8	h4	h2	h1	0~9	1-hour digit register
5	H_{10}	fr	PM/AM	h20	h10	0~1,2	10-hour digit register
6	D_1	d8	d4	d2	d1	0~9	1-day digit register
7	D_{10}	fr	*	d20	d10	0~3	10-day digit register
8	MO_1	mo8	mo4	mo2	mo1	0~9	1-month digit register
9	MO_{10}	fr	*	*	mo10	0~1	10-month digit register
A	Y_1	y8	y4	y2	y1	0~9	1-year digit register
B	Y_{10}	y80	y40	y20	y10	0~9	10-year digit register
C	W	fr	w4	w2	w1	0~6	Day-of-the-week register
D	C_D	30ADJ.	IRQ-F	CAL/HW	HOLD	–	Control register D
E	C_E	t1	t0	INT/STND	MASK	–	Control register E
F	C_F	TEST	24/12	STOP	RESET	–	Control register F

- The relation between register bit 0/1 and input/output is positive logic. 0 = Low; 1 = High.
- The count is in BCD code. For example, if the 1-year digit register (Y_1) is (y8, y4, y2, y1) = (0,0,1,0), the register indicates the "2" of "1992".
- Bits marked with * can be freely written to and used as RAM.
- A write instruction for the IRQ-F bit is not executed. This bit is set to "1" when the digit increment specified by t1,t0 is executed. The setting is maintained until the C_D register has been read, and then returns to "0".
- The fo (OSC FLAG) bit records any oscillation interruption. It is used to monitor for low battery voltage. The bit can be cleared by setting it to "0". (Setting the bit externally to "1" is also possible.)
- The fr (READ FLAG) bit goes to "0" when CE is set low, and goes to "1" when there is a carry to the seconds digit while a high signal is input to CE. This makes it possible to determine whether or not there was a carry to the seconds digit while the clock register was being read (i.e., while the CE input was high). If fr is "1", it is necessary to read the clock register again.
- The PM/AM bit is "1" for PM and "0" for AM.

6-2. Register Description

6-2-1. Clock/Calendar Register

(S_1,S_{10},MI_1,MI_{10},H_1,H_{10},D_1,D_{10},MO_1,MO_{10},Y_1,Y_{10},W)

- The register abbreviations stand for Second1, Second10, Minute1, Minute10, Hour1, Hour10, Day1, Day10, Month1, Month10, Year1, Year10, and Weekday. The notation is in BCD code, using numeric weighting.

- The registers are positive-logic registers. For example, (s8,s4,s2,s1) = 1001 means "9 seconds". Bits marked with* in the register table can be freely written to and used as RAM.

- Do not set impossible values to prevent the possibility of clock malfunction.

- Relation between PM/AM,h20,h10
  a) 12-hour notation
     Possible time settings are 12 a.m. to 11 a.m., and 12 p.m. to 11 p.m.
     The h20 bit cannot be written and is fixed to "0".
     The clock does not increment the h20 bit.
  24-hour notation
     Possible time settings are 0 to 23.
     A write attempt to the PM/AM bit is disregarded, and the bit will always read "0".

- Y_1,Y_{10} and leap years
  When using the western calendar, the last two digits of the year are assigned to Y_1 and Y_{10}. Leap years are determined by dividing the value indicated by Y_1 and $Y_{10}$by four; if the remainder is "0," the year is a leap year. Leap years are automatically determined in this manner, whether the year is numbered according to the western calendar or the Heisei nengo.
  Note : the year "99" is followed by "00".

- W register
  For this register, count-up from 0 to 6 is performed. The table below shows an example for bit weighting.

w4	w2	w1	Day of the week
0	0	0	Monday
0	0	1	Tuesday
0	1	0	Wednesday
0	1	1	Thursday
1	0	0	Friday
1	0	1	Saturday
1	1	0	Sunday

- fo flag (OSC FLAG)
  This bit records any oscillation interruption. It is used to monitor for low battery voltage. "1" means an oscillation interruption. The bit can be cleared by setting it to "0". It is also possible to externally set the bit to "1", but this should be avoided.

- fr (READ FLAG)
  The fr flag is set to "1" when there was a carry to the seconds value while the CE input was high. This flag makes it possible to determine whether or not a carry to the seconds value occurred while the clock register was being read (while the CE input was high). If the fr flag is "1", the entire clock register must be read again. The fr flag is cleared by setting CE low.

6-2-2. Control Registers

● CD register

Address	Register	D3	D2	D1	D0	
D	C_D	30ADJ.	IRQ-F	CAL/HW	HOLD	Control register D

• 30-second ADJ (30-second adjustment) bit

When this bit is written, it adjusts the time to 00 seconds when the seconds value for the current time is less than 30, and adjusts the time to 00 seconds and generates a carry to the minutes value when the seconds value for the current time is 30 or more. Because internal processing is being performed for 125 μs after this bit is written, do not write the S_1 to W registers and do not write a "1" to the RESET bit during this 125 μs interval.

This bit is maintained at "1" for 125 μs after it is written, and then is automatically reset to "0" afterwards. Therefore, confirm that the bit has been automatically reset to "0" before writing the S_1 to W registers.

• IRQ-F

IRQ-F goes to "1" and the STD.P output changes to low level according to the timing of the carry generation specified by the CE register bits t1 and t0 in combination.

a) During interrupt mode (INT/STD = "1")
   After IRQ-F goes to "1", IRQ-F is maintained at "1" until the CD register read is completed. After the CD register read is completed, IRQ-F is cleared to "0".
b) Constant cycle waveform output mode (INT/STD = "0")
   After approximately 7.8 ms, IRQ-F is automatically reset to "0". While IRQ-F is "1", the bit can also be cleared to "0" by reading the CD register.
   The carries can be generated at one of four rates, depending on the combination of t1 and t0: 64 Hz, 1 second, 1 minute, or 1 hour.

• CAL/HW (clock range switching bit)

When this bit is "1", the clock range is: seconds to the tens digit for years, and weeks
When this bit is "0", the clock range is: seconds to the tens digit for hours, and weeks
When this bit is "0", the six registers from D_1 to Y_{10} are not involved in clock operations, so they can be used as RAM for 4-bit data. The bits marked with asterisks and the fr flag portion of the D_{10} and MO_{10} registers can also be used as independent RAM.

• HOLD

This bit stops the 1-second digit incrementation. The clock continues to run, and the first incrementation after HOLD was set to "1" is compensated for when the hold condition is released (+1 second). The bit is cleared by writing "0".

●CE register

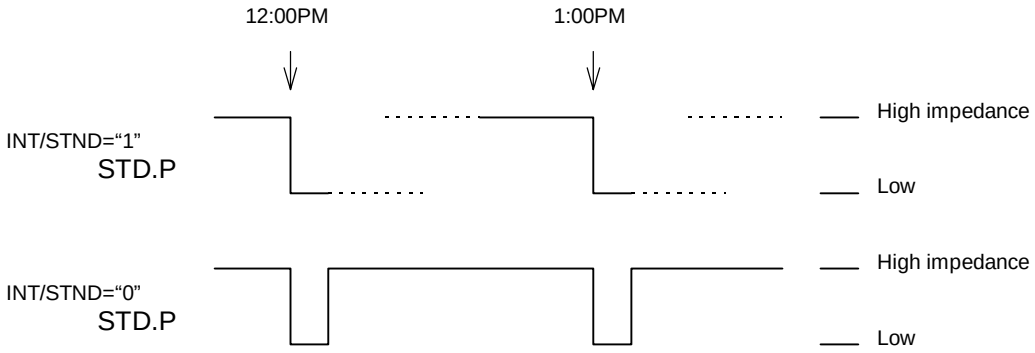
Address	Register	D3	D2	D1	D0	
E	C_E	t_1	t_0	INT/STND	MASK	Control register E

• t_1,t_0
Set the Period of the Periodic interrupt mode or fixed-period waveform mode.

t_1	t_0	Period
0	0	1/64 s
0	1	1 second
1	0	1 minute
1	1	1 hour

INT/STND bit = "1": interrupt mode
INT/STND bit = "0": fixed-period moveform output mode

Example t_1="1",t_0="1",MASK="0"

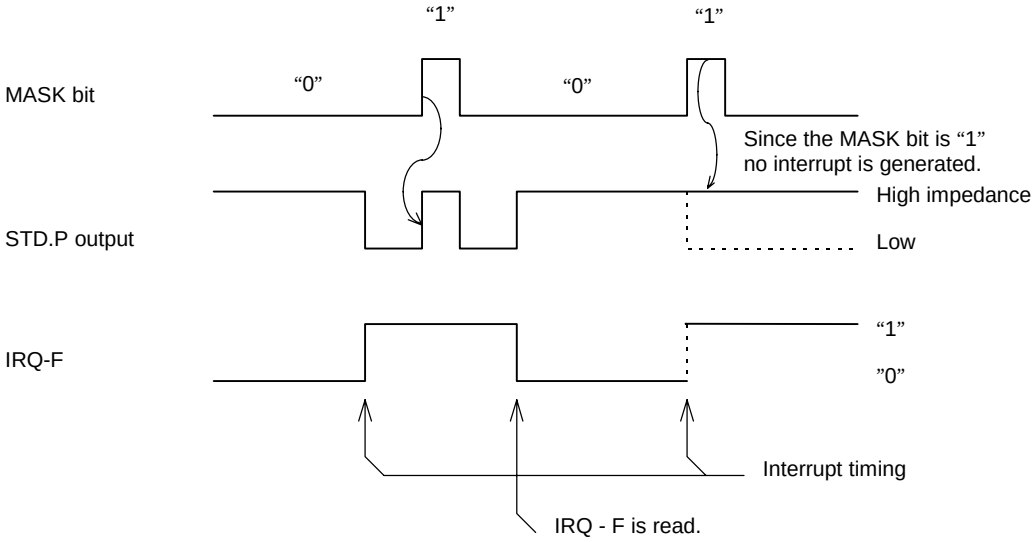


The fixed-period Low level cycle is 7.8 ms.
Because the 30-second adjustment could cause an incrementation, at the setting (t1,t0) = (1,0), (1,1) the STD.P output can become Low. If INT/STND = "0", the Low condition is maintained for up to 9.8 ms after the 30- second adjustment clear interval (after the 30-second ADJ flag has reverted to "0").
When the interrupt cycle is either 1 second, 1 minute, or 1 hour. If the HOLD bit is used to write S_1 - MI_{10}, and if there was an incrementation, the interrupt timing as determined by the incrementation is written to the S_1 - MI_{10} registers and will cause the STD.P output to be Low after the hold condition is released (IRQ-F becomes "1").
Except for the above case, writing the S_1 - H_1 registers has no effect on the STD.P output.

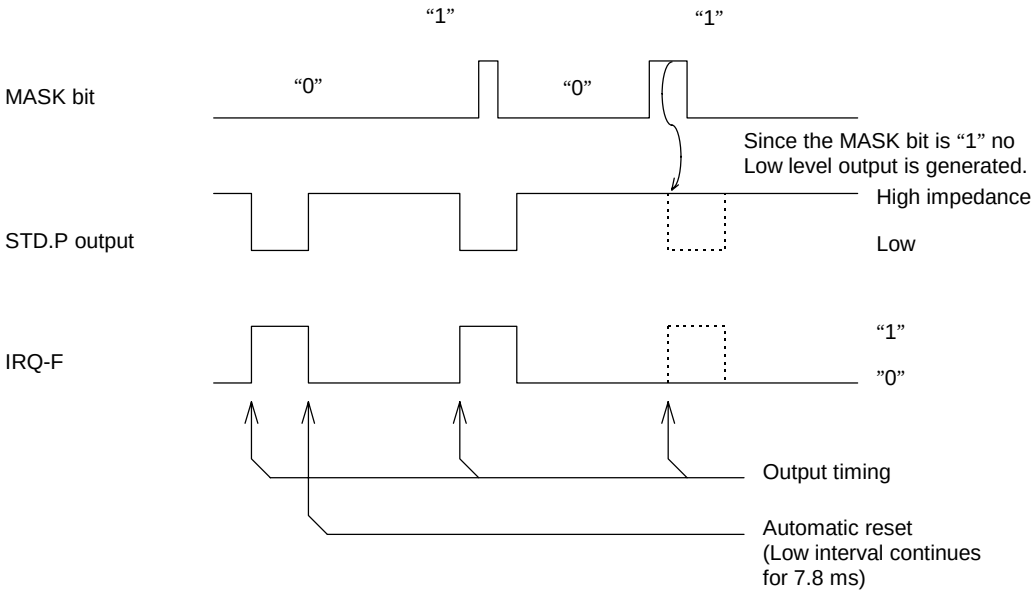
• INT/STND (interrupt/constant cycle waveform switching bit)
When this bit is "1", the "1" status of the IRQ-F bit and the Low condition of the STD.P output are maintained until the IRQ-F (C_D register) has been read.
When this bit is "0", the IRQ-F bit reverts to "0" after 7.8 ms or earlier if the IRQ-F bit is read before that. The Low level condition of the STD.P output reverts to high impedance after 7.8 ms.

- MASK
  When this bit is "1", IRQ-F cannot be "1" and the STD.P output is high impedance.

  Interrupt cycle mode (INT/STND = 1)



  Fixed-cycle mode (INT/STND = 0)



  If the IRQ-F bit is read, the bit is reset to "0" at that point. The STD.P output becomes Low for 7.8 ms and then is high impedance.

● CF register

Address	Register	D3	D2	D1	D0	
F	C_F	TEST	24/12	STOP	RESET	Control register F

- TEST
  This is a test bit for Epson's use. Always set this bit to "0". When writing other bits in the C_F register, be careful not to accidentally write a "1" to this bit. This bit is cleared when CE is set low.

- 24/12
  Selection bit for 12-hour or 24-hour notation. "1" means 24-hour and "0" means 12-hour notation. When this bit is changed, data above H_1 can become unstable and must be reset.

- STOP
  When this bit is set to "1", the clock stops. When the bit is set to "0", the clock resumes operation.

- RESET
  When this bit is set to "1", the seconds are reset to zero and the clock stops. This bit is cleared when CE is set low

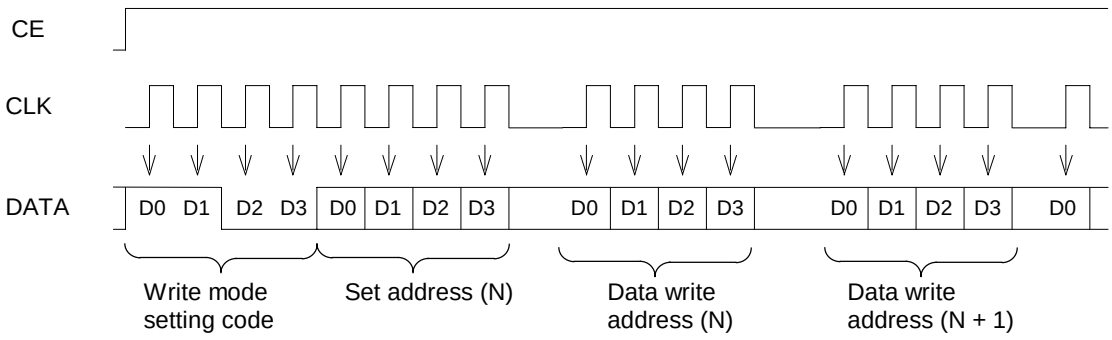
7. Usage

7-1. Function outline

Reads and writes are both performed in 4-bit units after the rising edge of the CE input. If the CE input falls before the input of the 4-bit units of data is completed, the four-bit write data being input at the moment the CE input fell is ignored. (The preceding data is valid, however.) Reads and writes are both performed LSB first.

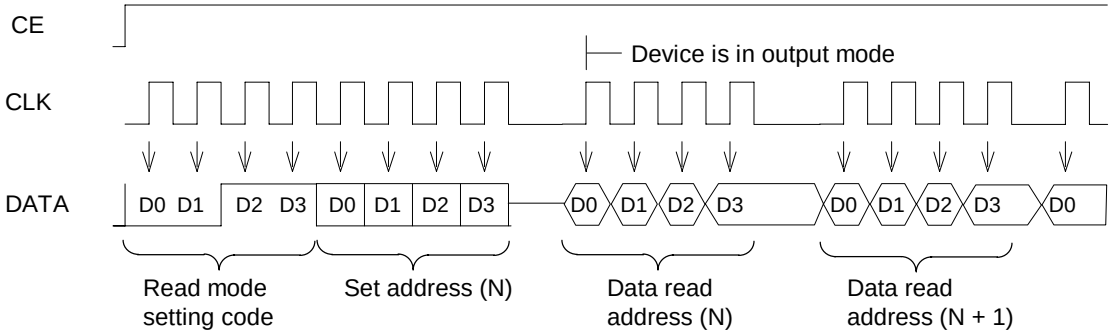
[Write operation]

1) After setting the CE input to High, make the first 4-bit block "3" to indicate write mode, and use the next 4-bit block to specify the address.
2) The following 4-bit block is written to the specified address. Then the address is automatically incremented, and subsequent 4-bit blocks are written to subsequent addresses.
3) The address incrementation is cyclic. After address F has been written, the selection returns to address 0.



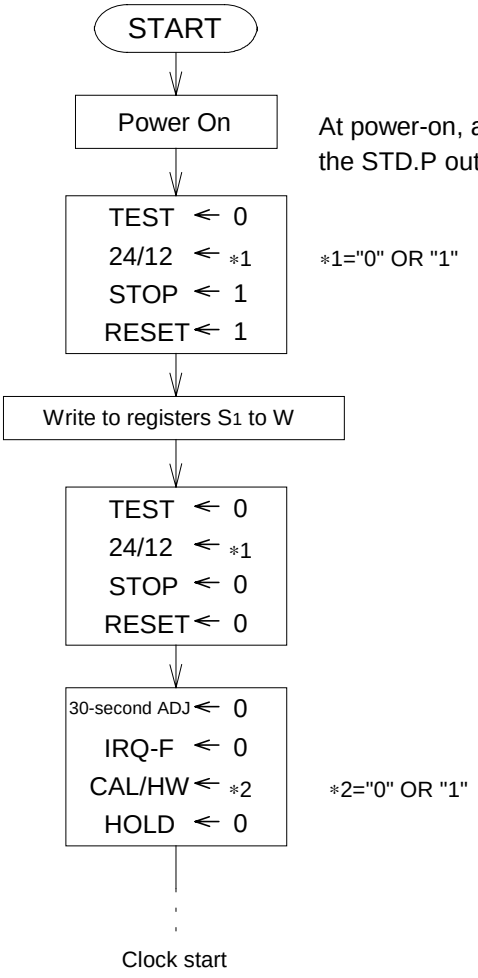
[Read operation]

1) After setting the CE input to High, make the first 4-bit block "C" to indicate read mode, and use the next 4-bit block to specify the address.
2) The four-bit data read that follows reads the data in the address that was set previously, and then the next four bits of data can be read from the automatically incremented address.



3) The address incrementation is cyclic. After address F has been read, the selection returns to address 0.
If the mode setting code is set to something other than "C" or "3", subsequent data are disregarded and the DATA port remains in the input mode.

7-2. Power-on procedure

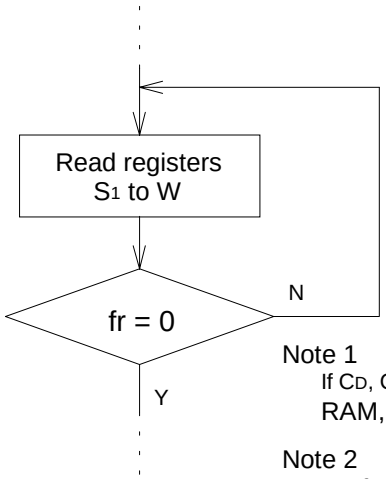


At power-on, all registers and the STD.P output are undefined.

*1="0" OR "1"

*2="0" OR "1"

7-3. Reading registers S_1 to W

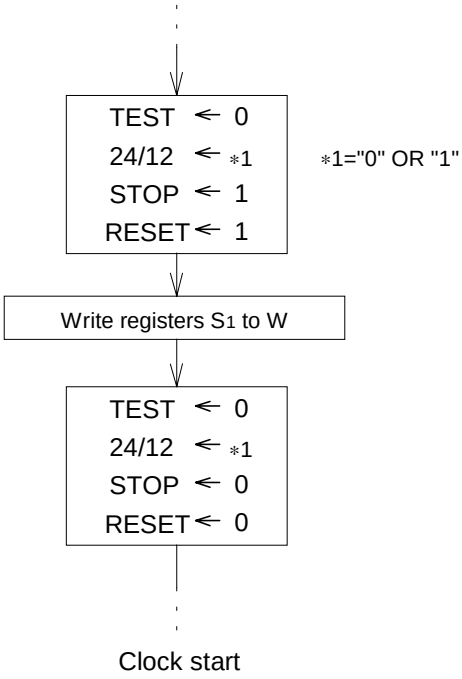


Note 1
If CD, CE, CF or registers S1 to W are used as RAM, the data can be read without using fr

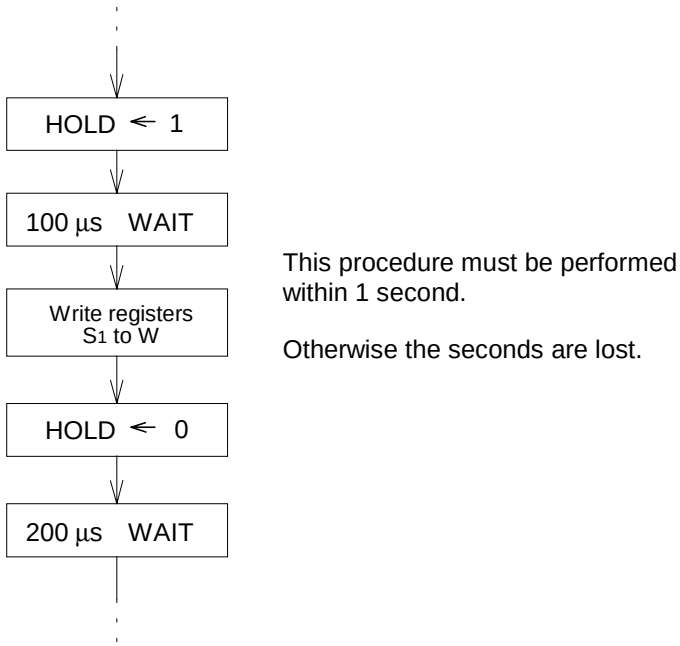
Note 2
Perform the fr check using the fr bit of the digit that was read last.

7-4. Writing registers S_1 - W

Method 1: No preservation of second data

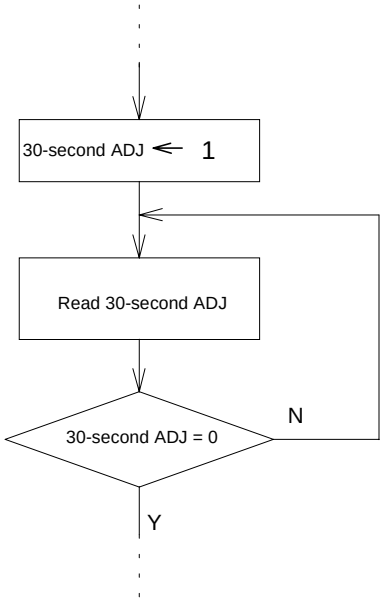


Method 2: Preservation of second data (for changeover to summer time)

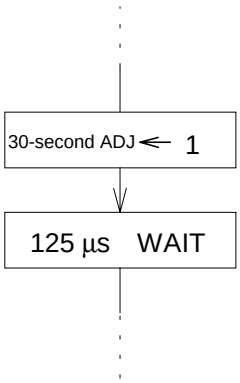


7-5. Writing the 30-second ADJ bit

Method 1



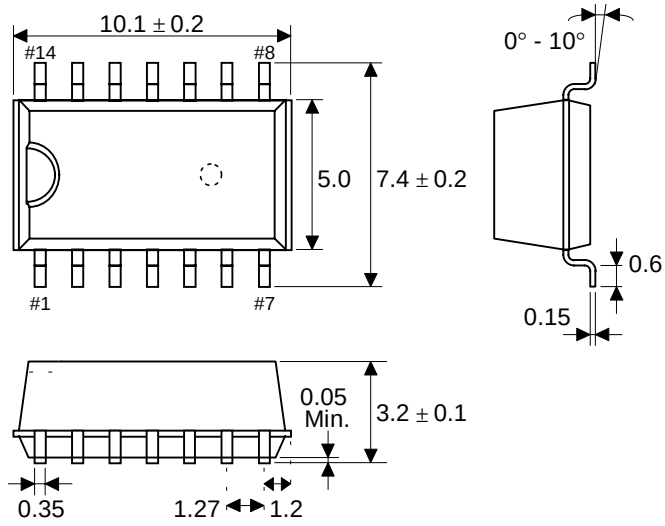
Method 2



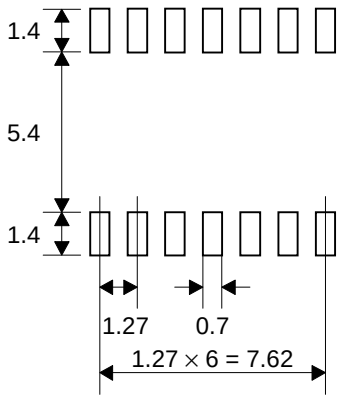
8. External Dimensions

RTC - 4513 (SOP-14pin)

•External dimensions



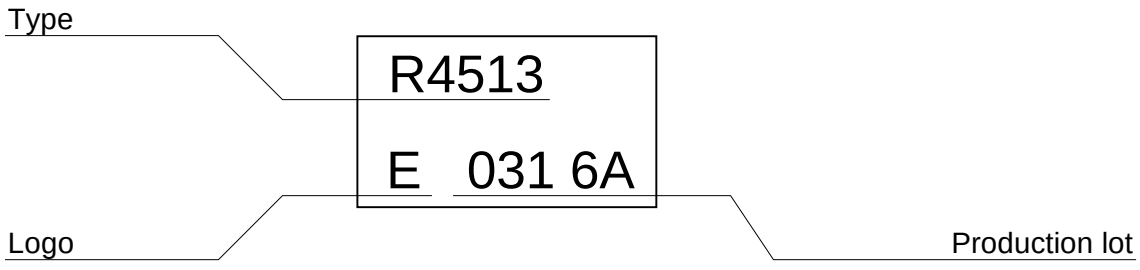
• Recommended solderring pattern



Unit : mm

9. Marking Layout

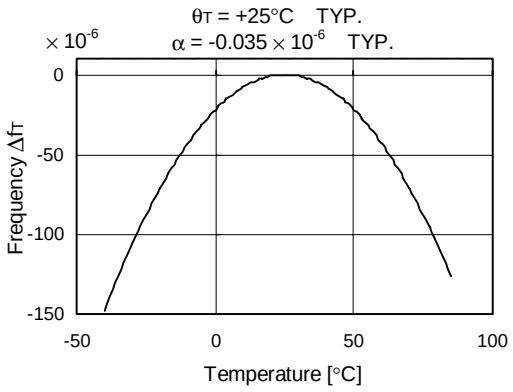
RTC - 4513 (SOP-14pin)



Note :
The above illustration is a general representation of the content and positioning of information on the chip.
It is not a detailed specification of the actual typeface, size or positioning.

10. Reference data

(1) Frequency temperature characteristics example



Finding the frequency stability (clock accuracy)

1. The frequency temperature characteristics can be approximated by using the following formula:

$\Delta fT = \alpha (\theta T - \theta X)^2$

ΔfT		: Frequency deviation at target temperature
α	(1 / °C^2)	: Secondary temperature coefficient ((-0.035±0.005) × 10^{-6} / °C^2)
θT	(°C)	: Peak temperature (+25±5 °C)
θX	(°C)	: Target temperature

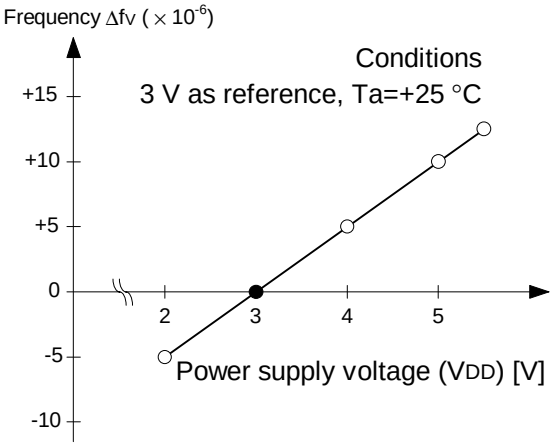
2. To determine the overall clock accuracy, add the frequency precision and the voltage characteristics:

$\Delta f/f = \Delta f/fo + \Delta fT + \Delta fV$

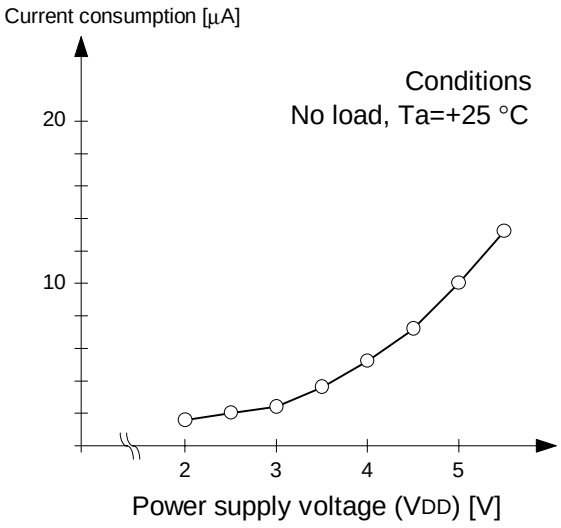
Δf/f	: Clock accuracy at a given temperature and voltage (frequency stability
Δf/fo	: Frequency precision
ΔfT	: Temperature dependent frequency deviation
ΔfV	: Voltage dependent frequency deviation

3. Finding the daily deviation:
Daily deviation = Δf/f × 86400(seconds)
The clock error is one second per day at 11.574 × 10^{-6}

(2) Example of the frequency/Voltage characteristic



(3) Example of the current consumption / voltage characteristics



Note:
These data show average values for a sample lot.

11. Application notes

11-1. Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1F as close as possible to the power supply pins (between V_{DD} and GNDs). Also, avoid placing any device that generates high level of electronic noise near this module.

* Do not connect signal lines to the shaded area in the figure shown in Fig. 1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

When the input pins are at the mid-level, this will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device. Therefore, try as much as possible to apply the voltage level close to V_{DD} or GND.

(4) Handling of unused pins

Since the input impedance of the input pins is extremely high, operating the device with these pins in the open circuit state can lead to unstable voltage level and malfunctions due to noise. Therefore, pull-up or pull-down resistors should be provided for all unused input pins.

11-2. Notes on packaging

(1) Soldering temperature conditions

If the temperature within the package exceeds 260, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

* See Fig. 2 for the soldering conditions of SMD products.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1: Example GND Pattern

RTC - 4513 (SOP-14pin)

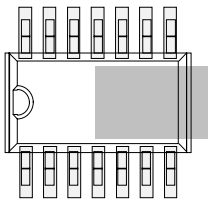
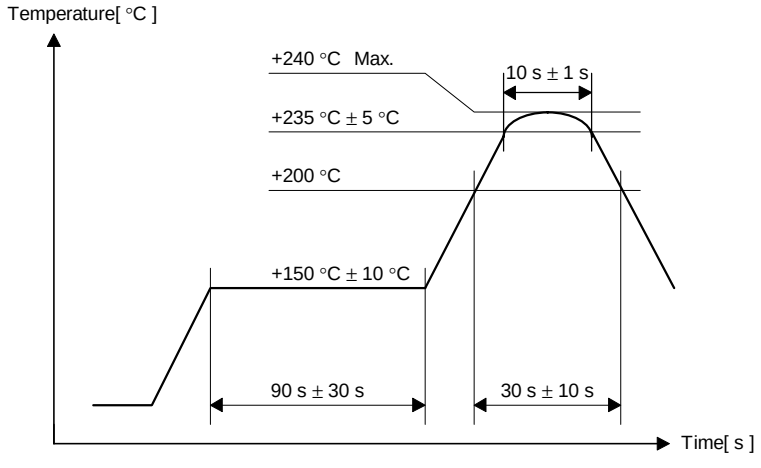


Fig. 2: Soldering Conditions of SMD Products
Air Reflow Profile



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