Evaluation Board

UDTech Taihu405EP

User's Manual

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Revision History

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1 Board Architecture

The PPC405EP contains a high-performance RISC processor core, on-chip memory, SDRAM controller, PCI bus interface, two Ethernet interfaces, control for external ROM and peripherals, DMA with scatter-gather support, two serial ports, an IIC interface, general purpose timers, and general purpose I/O. Utilizing this processor, features of the board include 128MB SDRAM, 2MB boot flash, 32MB flash for application, an IIC serial EEPROM stored the strap configuration data, a 32-bit PCI slot, a cardbus connector, a expansion interface connector (EBC connector), built-in Ethernet support, a USB device port, a 16X2 character LCD module, a CPLD, two serial ports, and a IIC serial temp&thermal monitor.

Figure 1-1 illustrates the board architecture, Subsequent paragraphs discuss aspects of the diagram in more detail.

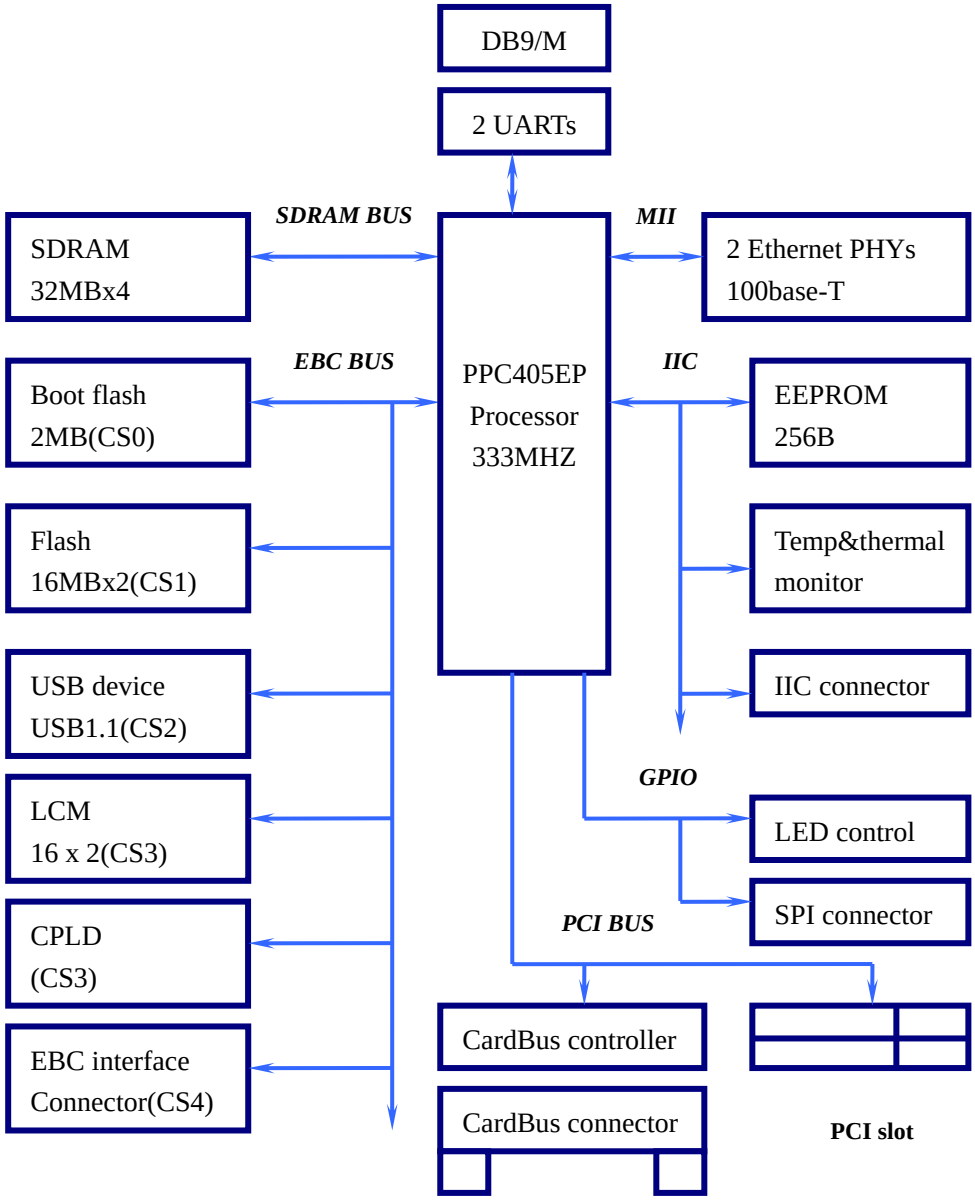

Figure 1-1. Board architecture

Figure 1-2 shows the top view board layout, the figure shows the headers unpopulated.

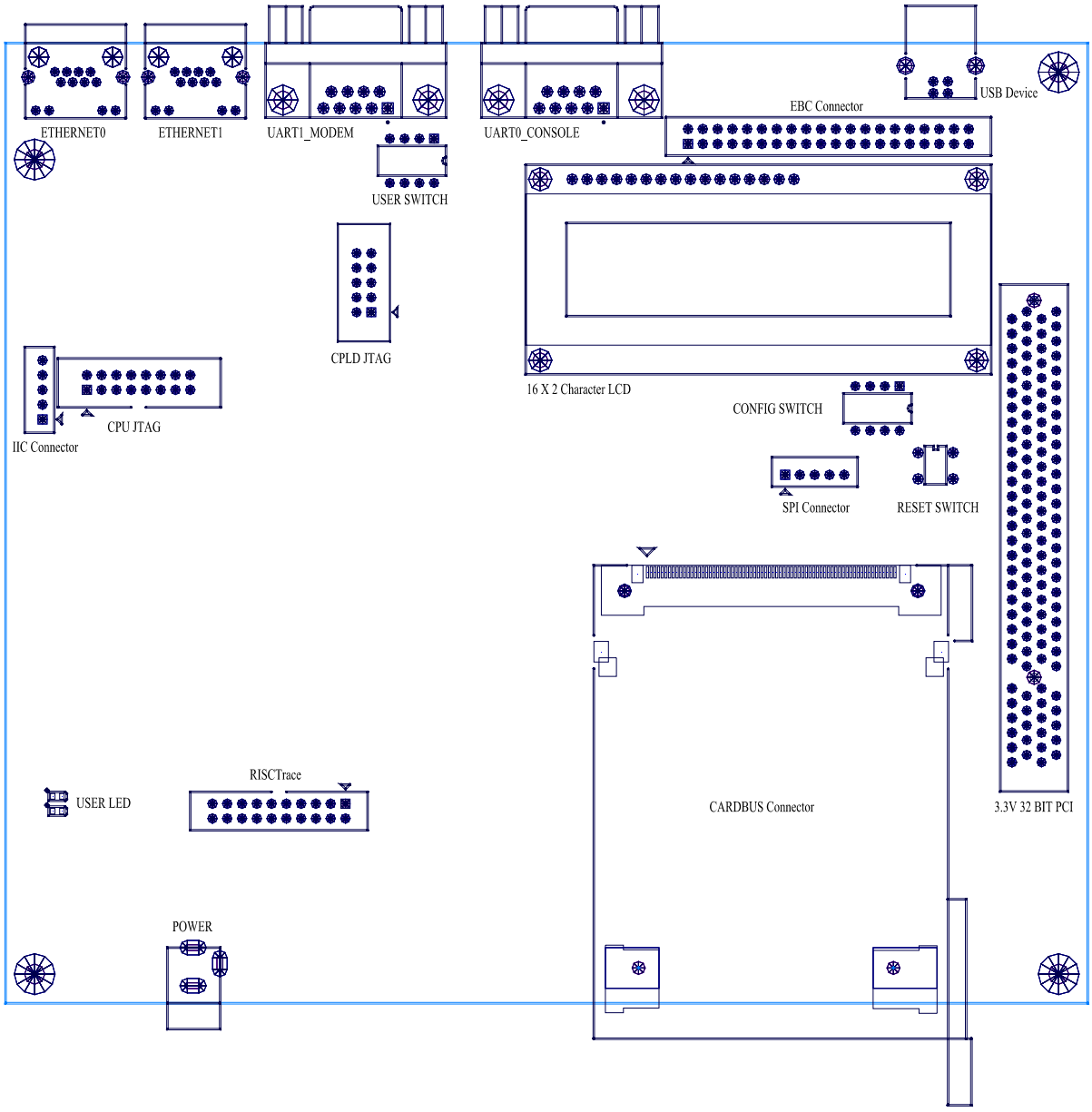

Figure 1-2. Top view board layout

1.1 Board Clocking

The clock architecture of the board is illustrated in figure 1-3. Note that the clock generator is reset only at board power-on, not by any other reset source.

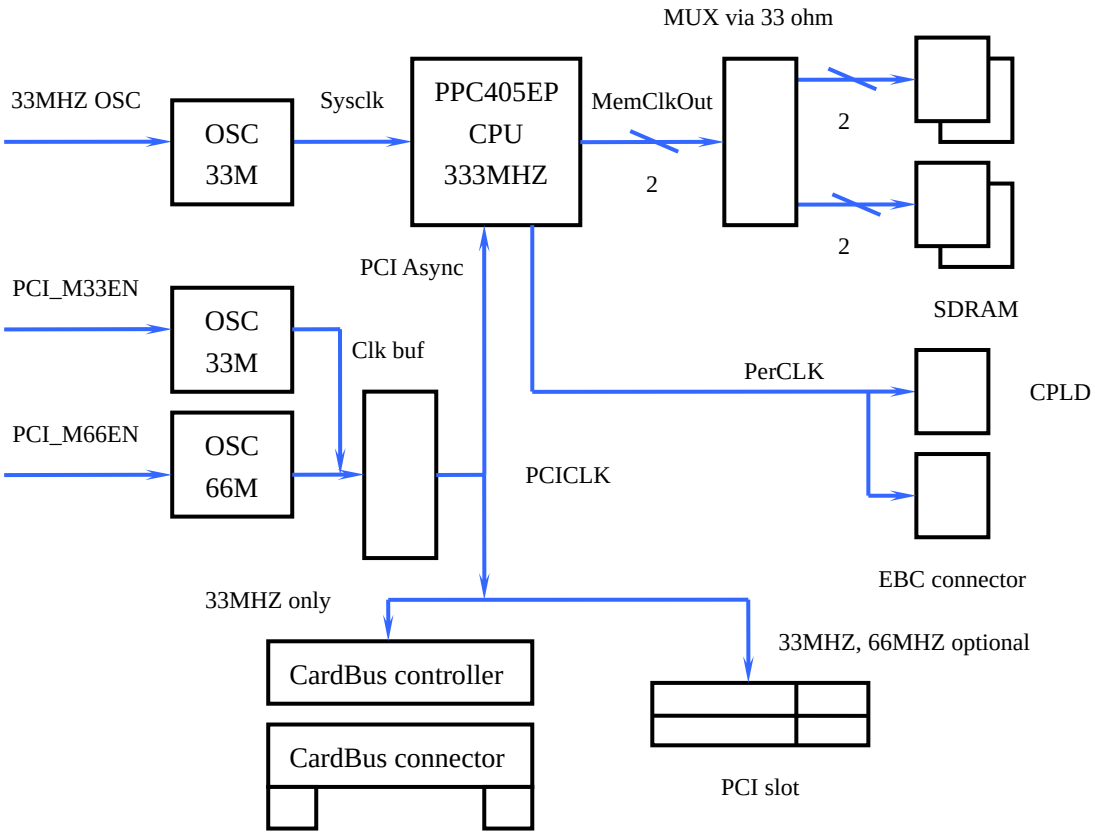

Figure 1-3. Clock architecture of the board

The PCI_M33EN and PCI_M66EN input to the OE (clock Output Enable) pin of the OSCs. And the PCI_M33EN is a NOT logic of the PCI_M66EN. The PCI_M66EN derives from an AND logic of the state of the M66EN pin on the PCI adapter interface and the state of the PCI_M66EN_hardwire position on the slide switch SW2. Note that the CardBus controller can't be functional when the 66MHZ clock is provided on the PCI adapter interface.

1.2 Strapping Options

The PPC405EP processor configures itself at reset based on strapping options. On the board, these options can be selected using slide switch SW2. In the design, the 66MHZ may be provided on the PCI adapter, but the on-chip synchronous PCI clock configuration for a 33 MHZ PCICLK differs from the configuration for a 66 MHZ PCICLK. So the strapping options for a 33MHZ PCICLK differ from the strapping options for a 66MHZ PCICLK.

The strapping options for the board are shown in Table 1-1. Table 1-1 shows the switching settings for

each option and the corresponding bits in the internal chip register (CPC0_BOOT) that are affected by the switch settings.

Table 1-1. Board Strapping Options

Switch (position)	Pin Name	CPC0_BOOT bits	Option
SW2(1)	**UART0_TX**	30 (SEEPROM Present)	Enable/Disable Configuration SEPROM 0 Disable (default) 1 Enable Because the serial EEPROM is present on the board, the PPC405EP can read configuration data from the serial EEPROM at IIC address 0b1010000 or be initialized through software. The default value is '0'.
SW2(2) & SW2(3)	**UART0_RTS & SYS_ERROR**	28:29 (ebcBootWidth)	If SW2(1) = 0 this is the Boot ROM width: 00 8 bits 01 16 bits(default) 10 Reserved 11 Reserved if PCI_M66EN = 0 or PCI_M66EN = 1, i.e. PCICLK = 33MHZ or PCICLK = 66MHZ, software must detect the state of PCI_M66EN and determine how the on-chip synchronous PCICLK is configured.
SW2(2) & SW2(3)	**UART0_RTS & SYS_ERROR**	25:26 (SEEPROM BaseAddress)	If SW2(1) = 1 this is the Boot ROM base address: 00 0x00(default) 01 0x40 10 0x80 11 0xC0 if PCI_M66EN = 0, the base address is 0x00(00). if PCI_M66EN = 1, the base address is 0x40(01). The configuration data of the two address space is different. The difference is how the on-chip synchronous PCICLK is configured.
SW2(4)	**PCI_M66EN _hardwire**		Enable/Disable 66MHZ PCICLK, the PCI_M66EN_hardwire is an input of the AND Gate which drives the PCI_M66EN. 0 Disable (default) 1 Enable

1.3 SDRAM Design

The PPC405EP chip supports 32-bit non-error correcting operation. On this board, SDRAM is provided by four chips which are addressed by two chip selects. Each of chip is 32MB.

The PPC405EP chip supports non-registered, non-buffered SDRAM at the processor local bus speed (up to 133 MHz). To achieve this bus speed and a CAS latency of 3 or less, it is required to use -75 or faster SDRAM. This corresponds to the normal PC-133 chip requirement for all SDRAM controllers. On the board, there are four clock inputs, each of which is separately driven.

1.4 PCI BUS

The PPC405EP chip supports an asynchronous 3.3V PCI bus at either 33MHz or 66MHz, or a 5V PCI bus at 33MHz. The board is provided with a standard 3.3V 32-bit PCI connector footprint. The board is also provided a CardBus connector footprint.

On this board, PCICLK input is selectable. A separate PCICLK input is also provided to PPC405EP. PCI bus frequencies up to 66MHz are supported. Normally, the PCI interface defaults to 33MHz if there are no PCI cards installed. Since the maximum PCI bus speed is 33MHz in a CardBus system, the CardBus controller can't be functional when the 66MHz clock is provided.

The PPC405EP PCI frequency range can be altered only at reset. It is set based upon the capability of the installed card. So the state of PCI_M66EN is provided to determine how to configure the on-chip synchronous PCICLK after reset. See *Table 1-1, "Board strapping Option*s", for more details.

The PPC405EP chip may be employed as either a PCI host or as a PCI adapter. This board demonstrates the host mode.

1.5 CardBus Controller

The CardBus controller used on the board is the Texas Instruments PCI1510PGE, a 144-terminal single-slot CardBus controller designed to meet the *PCI Bus Power Management Interface Specification for PCI to CardBus Bridges*, is an ultralow-power high-performance PCI-to-CardBus controller that supports a single PC card socket compliant with the *PC Card Standard* (rev. 7.2). The *PC Card Standard* retains the 16-bit PC Card specification defined in the *PCI Local Bus Specification* and defines the 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The controller supports Mix-and-match 5V/3.3V PC Cards and 3.3V CardBus Cards. A 3.3V CardBus connector is provided and 3.3V 32-bit CardBus Cards is supported fully on this board.

The Texas Instruments TPS2211AIDBR, single-slot PC Card power interface switch for parallel PCMCIA controllers, is used on the board. And the PCI1510PGE supports Parallel interface to TPS2211AIDBR single-slot PC Card power switch. The TPS2211AIDBR PC Card power interface switch provides an integrated power-management solution for a single PC Card. The chip allows the distribution

of 3.3V, 5V, and/or 12V card power, and is compatible with many PCMCIA controllers.

1.6 Ethernet Design

The board provides two 100Base-T Ethernet ports, with auto negotiation to 10Base-T when connected to networks not capable of 100Mbps operation.

Ethernet support through the Media Access Control (MAC) layer is provided in the PPC405EP chip. The Physical Layer Device (PHY) and the Physical Medium Dependent sublayer and interface (PMD) are provided on the board. The connections between the MAC and the PHY conform to the Medium Independent Interface (MII) specification.

The PHY and PMD sublayer are provided by a Realtek Semiconductor RTL8201BL. There are two PHYs, PHY0 and PHY1, provided. PHY0 is connected with address PHYAD=0b10100, and PHY1 is connected with address PHYAD=0b10000.

The supported media is Category 5 Unshielded Twisted Pair cable (UTP), accessed by means of RJ45 connectors on the board.

1.7 Flash Memory

Sixteen-bit flash is used on the board. There are 2MB boot flash and 32MB(2 pieces) application flash provided on the board. The PPC405EP boots from the 2MB flash which can be access by chip select PerCS0. Table 1-2 shows the chip select usage.

Table 1-2. Chip Select Usage

<table>
<tr><th>CS[4:0]</th><th colspan="2">Usage</th><th>Comment</th></tr>
<tr><td>PerCS0</td><td colspan="2">Boot flash</td><td>2MB</td></tr>
<tr><td>PerCS1</td><td colspan="2">Application flash</td><td>32MB(2 pieces)</td></tr>
<tr><td>PerCS2</td><td colspan="2">USB device</td><td>USB2.0, basic speed</td></tr>
<tr><td rowspan="3">PerCS3</td><td colspan="2">PerAddr30</td><td rowspan="3">The PerAddr30 determines which is selected between CPLD and LCM. The PerAddr[3:31] is peripheral address bus.
PerAddr30 PerAddr31
0 x CPLD
1 x LCM</td></tr>
<tr><td>0</td><td>CPLD</td></tr>
<tr><td>1</td><td>LCM</td></tr>
<tr><td>PerCS4</td><td colspan="2">EBC connector</td><td>2 x 20 Header</td></tr>
</table>

1.8 USB Device

The USB device controller used on the board is the Philips semiconductor PDIUSBD12. The PDIUSBD12 is a cost and feature optimized USB device. It communicates with the system processor over the high-speed general purpose parallel interface. To a processor, the PDIUSBD12 appears as a memory device with 8-bit data bus and 1 address bit (occupying 2 locations).

The PDIUSBD12 fully conforms to the USB specification Rev. 2.0 (basic speed). On this board, basic speed is supported.

1.9 16x2 Character LCD module

The 16X2 character LCD module (LCM) is provided on the board. It supports 16 columns by 2-line text display. And it includes a built-in 5 x 7 dot matrix font with the full range of ASCII characters. Backlighting may be turned on or off under program control.

The LCM communicates with the system processor over the general purpose parallel interface. It has 8-bit data bus and 1 address bit (occupying 2 locations) and shares PerCS3 with CPLD. See *Table 1-2, "Chip Select Usage"*, for more details.

1.10 CPLD

The CPLD is provided to read 4-position slide switch (SW1) status and detect the state of the PCI_M66EN. It finishes some distributed logic on the board. It communicates with the PPC405EP over the peripheral bus. See *Table 1-2, "Chip Select Usage"*, for more details.

Table 1-3 shows CPLD registers address assignment. Table 1-4 shows CPLD register0 usage. Table 1-5 shows CPLD register1 usage.

Table 1-3. CPLD Registers Address Assignment

A[30:31]	register	Comment
00	**Register0**	Reading the status
01	**Register1**	Writing control command

Table 1-4. CPLD Register0 Usage

D[7:0]	R/W	usage	Default	Comment
D0	**R**	**Ver0**	1	The board version number bit0
D1	**R**	**Ver1**	0	The board version number bit1
D2	**R**	**USB_SUSPEND**	0	USB Device suspend detecting
D3	**R**	**PCI_M66EN**	0	PCICLK 66MHz enable
D4	**R**	**SW1(1)**	0	4-position slide switch SW1
D5	**R**	**SW1(2)**	0	4-position slide switch SW1
D6	**R**	**SW1(3)**	0	4-position slide switch SW1
D7	**R**	**SW1(4)**	0	4-position slide switch SW1

Table 1-5. CPLD Register1 Usage

D[7:0]	R/W	usage	Default	Comment
D0	**R/W**	**Reserved**	0	
D1	**R/W**	**Reserved**	0	
D2	**R/W**	**Reserved**	0	
D3	**R/W**	**Reserved**	0	
D4	**R/W**	**Reserved**	0	
D5	**R/W**	**Reserved**	0	
D6	**R/W**	**LCM_CTRL**	0	LCM backlight control LCM_CTRL signal
D7	**R/W**	**USB_RESET**	1	USB device reset signal

1.11 GPIO Usage

The PPC405EP has one 32-bit GPIO controller. GPIO provides 32 user-programmable external signals, multiplexed with system-related signal groups including trace outputs, external interrupt inputs, chip selects, and UART interface signals. Table 1-6 shows the GPIO usage.

Table 1-6. GPIO Usage

GPIO[31:0]	Usage	Comment
GPIO0/PerBlast#	**GPIO0**	SPI port CS signal
GPIO1/TS1E	**TS1E**	RISCTrace port **TS1E** signal
GPIO2/TS2E	**TS2E**	RISCTrace port **TS2E** signal
GPIO3/TS1O	**TS1O**	RISCTrace port **TS1O** signal
GPIO4/TS2O	**TS2O**	RISCTrace port **TS2O** signal
GPIO5/TS3	**TS3**	RISCTrace port **TS3** signal
GPIO6/TS4	**TS4**	RISCTrace port **TS4** signal
GPIO7/TS5	**TS5**	RISCTrace port **TS5** signal
GPIO8/TS6	**TS6**	RISCTrace port **TS6** signal
GPIO9/TrcClk	**TrcClk**	RISCTrace port **TrcClk** signal
GPIO10/PerCS1#	**PerCS1#**	Chip select PerCS1
GPIO11/PerCS2#	**PerCS2#**	Chip select PerCS2
GPIO12/PerCS3#	**PerCS3#**	Chip select PerCS3
GPIO13/PerCS4#	**PerCS4#**	Chip select PerCS4
GPIO14/PerAddr03	**GPIO14**	SPI port SCLK signal
GPIO15/ PerAddr04	**GPIO15**	SPI port DI signal
GPIO16/ PerAddr05	**GPIO16**	SPI port DO signal
GPIO17/IRQ0	**IRQ0**	PCI slot interrupt request INTA
GPIO18/IRQ1	**IRQ1**	PCI slot interrupt request INTB
GPIO19/IRQ2	**IRQ2**	PCI slot interrupt request INTC
GPIO20/IRQ3	**IRQ3**	PCI slot interrupt request INTD
GPIO21/IRQ4	**IRQ4**	USB device interrupt request
GPIO22/IRQ5	**IRQ5**	EBC connector interrupt request
GPIO23/IRQ6	**UNUSED**	
GPIO24/UART0_DCD	**UART0_DCD**	UART1
GPIO25/UART0_DSR	**UART0_DSR**	UART1
GPIO26/UART0_RI	**UART0_RI**	UART1
GPIO27/UART0_DTR	**UART0_DTR**	UART1
GPIO28/UART1_RX	**UART1_RX**	UART0
GPIO29/ UART1_TX	**UART1_TX**	UART0
GPIO30/RejectPkt0	**GPIO30**	User programmable LED1 control signal
GPIO31/ RejectPkt0	**GPIO31**	User programmable LED2 control signal

1.12 Serial EEPROM

The Serial EEPROM (sEEPROM) used on the board is the ATMEL semiconductor AT24C02A. The AT24C02A provides 2048 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 256 words of 8 bits each. It is accessed via a Two-Wire (I2C) serial interface. The IIC address is 0x50. So the PPC405EP can read configuration data from the serial EEPROM after reset. Table 1-7 shows the IIC address usage on this board.

Table 1-7. IIC Address Usage

Device	IIC address	Comment
sEEPROM	**0x50**	Fixed
Temp&Thermal Monitor	**0x49**	
IIC Connector	**User defined**	

1.13 Temp&Thermal Monitor

The temp&thermal monitor used on the board is the MAXIM semiconductor DS1775R. The DS1775R Digital Thermometer and Thermostat provides temperature readings which indicate the temperature of the device. It measures temperatures from －55℃ to ＋125℃. Thermometer accuracy is ±2℃. It communicates with the PPC405EP over a Two-Wire (I2C) serial interface. The IIC address is 0x49. See *Table 1-7, "IIC Address Usage"*, for more detail.

1.14 Expansion Interface Support

A 2x20 header connector is provided to facilitate the attachment of customer prototyping logic. Some primary lines of External Peripheral interface are presented.

1.15 IIC Port Support

A 1x5 header connector is provided to connect to customer IIC devices.

1.16 SPI Port Support

A 1x5 header connector is provided on GPIOs. See Table 1-4, "GPIO Usage", for more details.

1.17 Serial Port

Two serial ports, software compatible with 16750, are included in the PPC405EP chip.

UART 1 provides a full set of modem control lines. Some of these lines are multiplexed with GPIO signals.

UART 0 provides only Tx and Rx.

1.18 Power Supply

There is universal 120/240V IN 5V/3A OUT power adapter.

1.19 PPC405EP Processor Power

The PPC405EP chip requires two voltages, +1.8V and +3.3V. In this board design, both voltages are derived from the +5V input. There are separate linear voltage regulators for each voltage.

2 Memory Map

Table 2-1 summarizes address space assignment on the board.

Table 2-1. PPC405EP Address Space assignment

Function	Subfunction	Start Address	End Address	Size
SDRAM bus	**SDRAM**	0x0000 0000	0x07FF FFFF	128MB
Peripheral bus	**USB Device (CS2)**	0x5000 0000	0x500F FFFF	1MB
	LCM&CPLD(CS3)	0x5010 0000	0x501F FFFF	1MB
	EBC connector(CS4)	0x5020 0000	0x502F FFFF	1MB
PCI	**PCI Memory**	0x8000 0000	0xE7FF FFFF	768MB
	PCI I/O	0xE800 0000	0xE800 FFFF	64KB
	PCI I/O	0xE880 0000	0xEBFF FFFF	56MB
	Configuration Registers	0xEEC0 0000	0xEEC0 0007	8B
	Interrupt Acknowledge and Special Cycle	0xEED0 0000	0xEED0 0003	4B
	Local Configuration Registers	0xEF40 0000	0xEF40 003F	64B
Internal peripherals	**GPT**	0xEF60 0000	0xEF60 00FF	256B
	UART0	0xEF60 0300	0xEF60 0307	8B
	UART1	0xEF60 0400	0xEF60 0407	8B
	IIC	0xEF60 0500	0xEF60 051F	32B
	OPB Arbiter	0xEF60 0600	0xEF60 063F	64B
	GPIO Controller Registers	0xEF60 0700	0xEF60 077F	128B
	Ethernet 0 Controller Registers	0xEF60 0800	0xEF60 08FF	256B
	Ethernet 1 Controller Registers	0xEF60 0900	0xEF60 09FF	256B
Peripheral bus	**Application Flash (CS1)**	0xFC00 0000	0xFDFF FFFF	32MB
Boot-up	**Boot Flash (CS0)**	0xFFE0 0000	0xFFFF FFFF	2MB

3 Programming the PPC405EP

This chapter provides guidance on programming the PPC405EP to work with the board design.

3.1 PLL Configuration

On this board, the 66MHz or 33MHz may be provided on the PCI adapter, but the on-chip synchronous PCI clock configuration for a 33 MHZ PCICLK differs from the configuration for a 66 MHZ PCICLK. Table 3-1 shows the PLL configuration difference between 33MHz PCICLK and 66MHz PCICLK. The input reference clock, SysCLk, derives from 33MHz OSC. Table 3-2 shows the clock configuration on the board.

Table 3-1. PLL Configuration

Core Clock	**266MHz**		**333MHz**	
On-chip PCICLK	**33MHz**	**66MHz**	**37MHz**	**111MHz**
CPC0_PLLMR0	0x0001 1003	0x0001 1001	0x0002 1002	0x0002 1000
CPC0_PLLMR1	0x8085 523E	0x8085 523E	0x80A5 52BE	0x80A5 52BE

Table 3-2. Clock Configuration

Core Clock	**266MHz**	**333MHz**
SDRAM Clock	**133MHZ**	**111MHZ**
Peripheral Clock	**66MHZ**	**55.5MHZ**
On-chip PCICLK	**33MHz or 66MHz**	**37MHz or 111MHZ**

3.2 SDRAM Bank 0-1

The SDRAM used on this board is the MICRON semiconductor MT48LC16M16A2. It is organized as 8,192 (13 bits) rows by 512 (9 bits) columns by 16 bits. Table 3-3 shows the SDRAM bank 0-1 configuration.

Table 3-3. SDRAM 0-1 Configuration

Registers	SDRAM(128MB)	
	Bank0	**Bank1**
SDRAM0_CFG	0x8080 0000	
SDRAM_B0CR	0x0008 4001	
SDRAM_B1CR		0x0408 4001
SDRAM0_TR	0x010B 4016	
SDRAM0_RTR	0x0330 0000	

3.3 Peripheral Bus Timings

The following timings all assume that the peripheral bus frequency is 66MHz. At lower bus frequencies, these timings should still work, though with sub-optimum throughput.

The EBC0_CFG register is same setting for five Peripheral banks. Table 3-4 show register EBC0_CFG setting.

Table 3-4. Register EBC0_CFG Setting

Initial	Bit	Field	Value	Description
0xC043 E000	**0**	**EBTC**	**1**	Between EBC transfers the peripheral data bus, address bus and control signals are driven.
	1	**PTD**	**1**	Disable time-outs
	2:4	**RTC**	**000**	When PTD=0, the number of cycles from PerAddr3:31 changing until a timeout error occurs.
	5:8			Reserved.
	9	**CSTC**	**1**	PerCS0:4 are always driven.
	10:11	**BPF**	**00**	Burst prefetch 1 doubleword.
	12:13			Reserved.
	14	**PME**	**1**	Power management enable
	15:18	**PMT**	**1111**	The EBC makes a sleep request to the Clock and the EBC has been idle for 32 x 15 PerClk cycles.
	20:31			Reserved.

3.3.1 Peripheral Bank 0

The boot flash, 2MB, is attached to bank 0. Table 3-5 show Peripheral bank 0 register **EBC0_B0CR** settings. Table 3-6 show Peripheral bank 0 register **EBC0_B0AP** settings.

Table 3-5. Register EBC0_B0CR Setting

Initial	Bit	Field	Value	Description
0xFFE3 A000	**0:11**	**BAS**	**0xFFE**	The bank 0 base address is 0xFFE.
	12:14	**BS**	**001**	The bank 0 size is 2MB.
	15:16	**BU**	**11**	Read/write can be allowed for the bank 0.
	17:18	**BW**	**01**	The bank 0 bus width is 16-bit.
	19:31			Reserved.

Table 3-6. Register EBC0_B0AP Setting

Initial	Bit	Field	Value	Description
0x0381 5600	**0**	**BME**	**0**	Burst mode disable.
	1:8	**TWT**	**0000 0111**	Transfer waits 7 PerCLK cycles.
	9:11			Reserved.
	12:13	**CSN**	**00**	Number of cycles from peripheral address driven to PerCS0 low.
	14:15	**OEN**	**01**	Number of cycles from PerCS0 low to PerOE low.
	16:17	**WBN**	**01**	Number of cycles from PerCS0 low to PerWBE0:1 active.
	18:19	**WBF**	**01**	Number of cycles PerWBE0:1 becomes inactive prior to PerCS0 inactive.
	20:22	**TH**	**011**	Contains the number of hold cycles inserted at the end of a transfer.
	23	**RE**	**0**	PerReady is disabled.
	24	**SOR**	**0**	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	**BEM**	**0**	PerWBE0:1 is only active for write cycles.
	26:31			Reserved.

3.3.2 Peripheral Bank 1

The application flash, 32MB, is attached to bank 1. Table 3-7 show Peripheral bank 1 register **EBC0_B1CR** settings. Table 3-8 show Peripheral bank 1 register **EBC0_B1AP** settings.

Table 3-7. Register EBC0_B1CR Setting

Initial	Bit	Field	Value	Description
0xFC0B A000	**0:11**	**BAS**	**0xFC0**	The bank 1 base address is 0xFD0.
	12:14	**BS**	**101**	The bank 1 size is 32MB.
	15:16	**BU**	**11**	Read/write can be allowed for the bank 1.
	17:18	**BW**	**01**	The bank 1 bus width is 16-bit.
	19:31			Reserved.

Table 3-8. Register EBC0_B1AP Setting

Initial	Bit	Field	Value	Description
0x0581 5600	**0**	**BME**	**0**	Burst mode disable.
	1:8	**TWT**	**0000 1011**	Transfer waits 11 PerCLK cycles.
	9:11			Reserved.
	12:13	**CSN**	**00**	Number of cycles from peripheral address driven to PerCS1 low.
	14:15	**OEN**	**01**	Number of cycles from PerCS1 low to PerOE low.
	16:17	**WBN**	**01**	Number of cycles from PerCS1 low to PerWBE0:1 active.
	18:19	**WBF**	**01**	Number of cycles PerWBE0:1 becomes inactive prior to PerCS1 inactive.
	20:22	**TH**	**011**	Contains the number of hold cycles inserted at the end of a transfer.
	23	**RE**	**0**	PerReady is disabled.
	24	**SOR**	**0**	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	**BEM**	**0**	PerWBE0:1 is only active for write cycles.
	26:31			Reserved.

3.3.3 Peripheral Bank 2

The USB device is attached to bank 2. Table 3-9 show Peripheral bank 2 register **EBC0_B2CR** settings. Table 3-10 show Peripheral bank 2 register **EBC0_B2AP** settings.

Table 3-9. Register EBC0_B2CR Setting

Initial	Bit	Field	Value	Description
0x5001 8000	**0:11**	**BAS**	**0x500**	The bank 2 base address is 0x500.
	12:14	**BS**	**000**	The bank 2 size is 1MB.
	15:16	**BU**	**11**	Read/write can be allowed for the bank 2.
	17:18	**BW**	**00**	The bank 2 bus width is 8-bit.
	19:31			Reserved.

Table 3-10. Register EBC0_B2AP Setting

Initial	Bit	Field	Value	Description
0x0301 6600	**0**	**BME**	**0**	Burst mode disable.
	1:8	**TWT**	**0000** **0110**	Transfer waits 6 PerCLK cycles.
	9:11			Reserved.
	12:13	**CSN**	**00**	Number of cycles from peripheral address driven to PerCS2 low.
	14:15	**OEN**	**01**	Number of cycles from PerCS2 low to PerOE low.
	16:17	**WBN**	**01**	Number of cycles from PerCS2 low to PerWBE0:1 active.
	18:19	**WBF**	**10**	Number of cycles PerWBE0:1 becomes inactive prior to PerCS2 inactive.
	20:22	**TH**	**011**	Contains the number of hold cycles inserted at the end of a transfer.
	23	**RE**	**0**	PerReady is disabled.
	24	**SOR**	**0**	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	**BEM**	**0**	PerWBE0:1 is only active for write cycles.
	26:31			Reserved.

3.3.4 Peripheral Bank 3

The LCM and CPLD are attached to bank 3. Table 3-11 show Peripheral bank 3 register **EBC0_B3CR** settings. Table 3-12 show Peripheral bank 3 register **EBC0_B3AP** settings.

Table 3-11. Register EBC0_B3CR Setting

Initial	Bit	Field	Value	Description
0x5011 8000	**0:11**	**BAS**	**0x501**	The bank 3 base address is 0x501.
	12:14	**BS**	**000**	The bank 3 size is 1MB.
	15:16	**BU**	**11**	Read/write can be allowed for the bank 3.
	17:18	**BW**	**00**	The bank 3 bus width is 8-bit.
	19:31			Reserved.

Table 3-12. Register EBC0_B3AP Setting

Initial	Bit	Field	Value	Description
0x158F F600	**0**	**BME**	**0**	Burst mode disable.
	1:8	**TWT**	**0010 1011**	Transfer waits 43 PerCLK cycles.
	9:11			Reserved.
	12:13	**CSN**	**11**	Number of cycles from peripheral address driven to PerCS3 low.
	14:15	**OEN**	**11**	Number of cycles from PerCS3 low to PerOE low.
	16:17	**WBN**	**11**	Number of cycles from PerCS3 low to PerWBE0:1 active.
	18:19	**WBF**	**11**	Number of cycles PerWBE0:1 becomes inactive prior to PerCS3 inactive.
	20:22	**TH**	**011**	Contains the number of hold cycles inserted at the end of a transfer.
	23	**RE**	**0**	PerReady is disabled.
	24	**SOR**	**0**	Data transfer occurs one PerClk cycle after PerReady is sampled active.
	25	**BEM**	**0**	PerWBE0:1 is only active for write cycles.
	26:31			Reserved.

3.3.5 Peripheral Bank 4

The expansion interface connector is attached to bank 4. If the customer logic is not installed, the bank 4 is disabled. Table 3-13 show Peripheral bank 4 register settings.

Table 3-13. Peripheral bank 4 register settings

Registers	EBC connector (not installed), PerCS4
EBC0_B4CR	**0x5020 2000**
EBC0_B4AP	

4 Reset and Interrupts

Reset is generated at power-on, by the reset pushbutton, by system-reset from the PPC405EP or by undervoltage on either the +5V or +3.3V supplies.

There are 7 external interrupt inputs to the PPC405EP. They are multiplexed with GPIOs. More detail about these interrupts is given in *Table 1-6, "GPIO Usage"*.

5 Switches

The board contains a reset switch and a 4-position slide switch for testing. Additionally, the board contains a 4-position slide switch for setting the configuration of the PPC405EP chip and certain board functions. Table 5-1 shows the switch list.

Table 5-1. Switch List

Location	Function
SW1	**Testing Switch**
SW2	**PPC405EP and Board Strapping Switch**
SW3	**Reset Pushbutton Switch**

6 Displays

The LED displays provided on the board are described in Table 6-1.

Table 6-1. Displays

Name	Location	Color	Description
Power Present	**LD3**	**Green**	Lights when the Power Adapter is installed
Power Good	**LD2**	**Red**	Lights when the +3.3V voltage is supplied
Flash Status	**LD7**	**Green**	Lights when the flash is busy
USB Goodlink	**LD1**	**Red**	USB Goodlink LED indicator
Cardbus Card Present	**LD10**	**Green**	Lights when the Cardbus card is installed
Cardbus Card Goodlink	**LD11**	**Red**	Cardbus interface link status
PHY0 Full Duplex	**LD5**	**Green**	Lights to indicator PHY0 full duplex mode for Ethernet
Ethernet PHY0 Status	**JT1**	**Yellow–Tx/Rx Activity Green–Link Status**	Dual LEDs, part of the RJ-45 PHY1 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.
PHY1 Full Duplex	**LD6**	**Green**	Lights to indicator PHY1 full duplex mode for Ethernet
Ethernet PHY1 Status	**JT2**	**Yellow–Tx/Rx Activity Green–Link Status**	Dual LEDs, part of the RJ-45 PHY1 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.
Machine Check	**LD4**	**Red**	Lights when the PPC405EP SYS_ERROR signal is asserted.
LED1	**LD9**	**Green**	User programmable LED1
LED2	**LD8**	**Green**	User programmable LED2

7 Connectors

The connector types and pin usage for board connectors are described in the following sections. Table 7-1 shows the switch list.

Table 7-1. Connector List

Location	Description
JT1	**PHY0 Ethernet TWP connector**
JT2	**PHY1 Ethernet TWP connector**
JT3	**USB device up-plug type A connector**
JT4	**Serial port 1 connector**
JT5	**Serial port 0 connector**
JT6	**EBC connector**
JT7	**CPLD JTAG Port**
JT8	**JTAG Debugger connector**
JT9	**IIC connector**
JT10	**SPI connector**
JT11	**Cardbus connector**
JT12	**PCI connector**
JT13	**RISCTrace connector**
JT14	**The power adapter connector**

7.1 Expansion Interface Connector

User logic may be placed on a daughter card attached to the Expansion Interface connector. The pin usage of the connector is described in Table 7-2. Refer to the board schematic for the definitions of each of the signal names in the table.

Table 7-2. Expansion Interface Connector Pin Assignment

Pin	Signal name	Pin	Signal name
1	EBC_D7	2	EBC_A7
3	EBC_D6	4	EBC_A6
5	EBC_D5	6	EBC_A5
7	EBC_D4	8	EBC_A4
9	EBC_D3	10	EBC_A3
11	EBC_D2	12	EBC_A2
13	EBC_D1	14	EBC_A1
15	EBC_D0	16	EBC_A0
17	3.3VCC	18	3.3VCC
19	GND	20	GND
21	EBC_D15	22	EBC_CLK
23	EBC_D14	24	GND
25	EBC_D13	26	EBC_RESET
27	EBC_D12	28	EBC_WE
29	EBC_D11	30	EBC_OE
31	EBC_D10	32	EBC_CS4
33	EBC_D9	34	EBC_WBE0
35	EBC_D8	36	EBC_IRQ4
37	GND	38	GND
39	5.0VCC	40	5.0VCC

7.2 IIC Connector

The IIC connects to a 1x5 header connector. The pin assignment of the connector is described in Table 7-3.

Table 7-3. IIC Connector Pin Assignment

Pin	Signal name
1	GND
2	IICSCL
3	IICSDA
4	GND
5	GND

7.3 SPI Connector

The SPI connects to a 1x5 header connector. The pin assignment of the connector is described in Table 7-4.

Table 7-4. SPI Connector Pin Assignment

Pin	Signal name
1	SPI_CS
2	SPI_DI
3	SPI_DO
4	GND
5	SPI_SCLK

7.4 JTAG Debugger Connector

The JTAG debugger connects to the board through a 2x8-pin header. Pin usage is described in Table 7-5.

Table 7-5. JTAG Debugger Connector Pin Assignment

Pin	Signal name
1	**TDO**
2	**Unused**
3	**TDI**
4	**TRST,** from BDI2000
5	**Unused**
6	**Power,** This is a status signal, not a power source.
7	**TCK**
8	**Unused**
9	**TMS**
10	**Unused**
11	**HALT,** from BDI2000
12	**Unused**
13	**Unused**
14	**Unused**
15	**Unused**
16	**GND**

7.5 RISCTrace Connector

The RISCTrace feature connects to the board through a 2x10-pin header. Pin usage is described in Table 7-6.

Table 7-6. RISCTrace Connector Pin Assignment

Pin	Signal name
1	Reserved
2	Reserved
3	TrcCLK
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	TS1O
13	TS2O
14	TS1E
15	TS2E
16	TS3
17	TS4
18	TS5
19	TS6
20	GND

7.6 Serial Port Connector

Two serial ports are included on the board. Pin usage is described in Table 7-7.

Table 7-7. Connector List

Pin	Signal name	Serial 0	Serial 1	Comment
1	DCD#		√	Carrier Detect
2	RXD	√	√	Receive Data
3	TXD	√	√	Transmit Data
4	DTR#		√	Data Terminal Ready
5	GND	√	√	System Ground
6	DSR#		√	Data Set Ready
7	RTS#		√	Request to Send
8	CTS#		√	Clear to Send
9	RI#		√	Ring Indicator

7.7 CPLD JTAG Connector

The CPLD may be programmed in place on the board via this JTAG connector and appropriate downloading software. It is a 2x5 header connector. The pin assignment of the connector is described in Table 7-8.

Table 7-8. CPLD JTAG Connector Pin Assignment

Pin	Signal name
1	TCK
2	GND
3	TDO
4	3.3V
5	TMS
6	Unused
7	Unused
8	Unused
9	TDI
10	GND

7.8 PCI Connector

PCI slot is a standard 4 x 30, 2 millimeter connector as defined by the +3.3VDC, 32-bit, 62-pin, PCI edge specification. This interface allows PCI cards to be interfaced to the evaluation board. The pin assignment of the connector is described in Table 7-9.

Table 7-9. PCI Connector Pin Assignment

Pin (component)	Signal name	Pin	Signal name
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	Reserved
B10	Reserved	A10	+3.3V(I/O)
B11	PRSNT2#	A11	Reserved
B12	KEY	A12	KEY

B13	**KEY**	**A13**	**KEY**
B14	**Reserved**	**A14**	**3.3Vaux**
B15	**GND**	**A15**	**RST#**
B16	**CLK**	**A16**	**+3.3V(I/O)**
B17	**GND**	**A17**	**GNT#**
B18	**REQ#**	**A18**	**GND**
B19	**+3.3V(I/O)**	**A19**	**PME#**
B20	**AD31**	**A20**	**AD30**
B21	**AD29**	**A21**	**+3.3V**
B22	**GND**	**A22**	**AD28**
B23	**AD27**	**A23**	**AD26**
B24	**AD25**	**A24**	**GND**
B25	**+3.3V**	**A25**	**AD24**
B26	**C/BE3#**	**A26**	**IDSEL**
B27	**AD23**	**A27**	**+3.3V**
B28	**GND**	**A28**	**AD22**
B29	**AD21**	**A29**	**AD20**
B30	**AD19**	**A30**	**GND**
B31	**+3.3V**	**A31**	**AD18**
B32	**AD17**	**A32**	**AD16**
B33	**C/BE2#**	**A33**	**+3.3V**
B34	**GND**	**A34**	**FRAME#**
B35	**IRDY#**	**A35**	**GND**
B36	**+3.3V**	**A36**	**TRDY#**
B37	**DEVSEL#**	**A37**	**GND**
B38	**GND**	**A38**	**STOP**
B39	**LOCK#**	**A39**	**+3.3V**
B40	**PERR#**	**A40**	**+3.3V**
B41	**+3.3V**	**A41**	**+3.3V**
B42	**SERR#**	**A42**	**GND**
B43	**+3.3V**	**A43**	**PAR**
B44	**C/BE1#**	**A44**	**AD15**
B45	**AD14**	**A45**	**+3.3V**
B46	**GND**	**A46**	**AD13**
B47	**AD12**	**A47**	**AD11**
B48	**AD10**	**A48**	**GND**
B49	**M66EN**	**A49**	**AD9**
B50	**GND**	**A50**	**GND**
B51	**GND**	**A51**	**GND**
B52	**AD8**	**A52**	**C/BE0#**
B53	**AD7**	**A53**	**+3.3V**
B54	**+3.3V**	**A54**	**AD6**

B55	**AD5**	**A55**	**AD4**
B56	**AD3**	**A56**	**GND**
B57	**GND**	**A57**	**AD2**
B58	**AD1**	**A58**	**AD0**
B59	**+3.3V(I/O)**	**A59**	**+3.3V(I/O)**
B60	**ACK64#**	**A60**	**REQ64#**
B61	**+5V**	**A61**	**+5V**
B62	**+5V**	**A62**	**+5V**

7.9 CARDBUS Connector

The CARDBUS connector is a 68-pin SMT connector. The pin assignment of the connector is described in Table 7-10.

Table 7-10. CARDBUS Connector Pin Assignment

Pin	Signal name
1	**GND**
2	**CAD0**
3	**CAD1**
4	**CAD3**
5	**CAD5**
6	**CAD7**
7	**CCBE0#**
8	**CAD9**
9	**CAD11**
10	**CAD12**
11	**CAD14**
12	**CCBE1#**
13	**CPAR**
14	**CPERR#**
15	**CGNT#**
16	**CINT#**
17	**VCC**
18	**VPP1**
19	**CCLK**
20	**CIRDY#**
21	**CCBE2#**
22	**CAD18**
23	**CAD20**
24	**CAD21**
25	**CAD22**

26	**CAD23**
27	**CAD24**
28	**CAD25**
29	**CAD26**
30	**CAD27**
31	**CAD29**
32	**Reserved**
33	**CCLKRUN#**
34	**GND**
35	**GND**
36	**CCD1#**
37	**CAD2**
38	**CAD4**
39	**CAD6**
40	**Reserved**
41	**CAD8**
42	**CAD10**
43	**CVS1**
44	**CAD13**
45	**CAD15**
46	**CAD16**
47	**Reserved**
48	**CBLOCK#**
49	**CSTOP#**
50	**CDEVSEL#**
51	**VCC**
52	**VPP2**
53	**CTRDY#**
54	**CFRAME#**
55	**CAD17**
56	**CAD19**
57	**CVS2**
58	**CRST#**
59	**CSERR#**
60	**CREQ#**
61	**CCBE3#**
62	**CAUDIO**
63	**CSTSCHG**
64	**CAD28**
65	**CAD30**
66	**CAD31**
67	**CCD2#**
68	**GND**

8 Board Dimension

Figures 8-1 shows the dimension for the evaluation board.

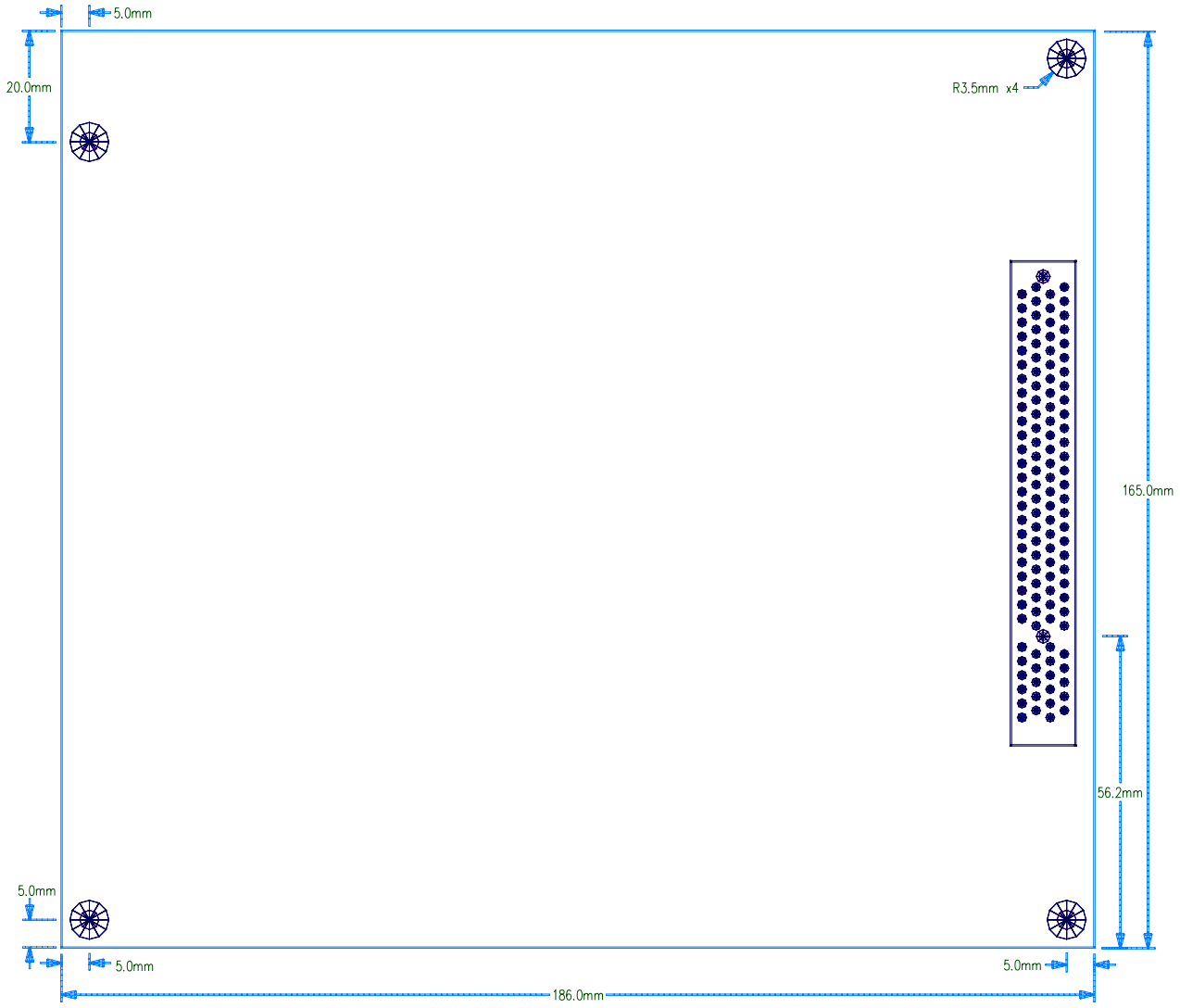

Figure 8-1. The evaluation board dimension

9 CPLD Programming

The following section contains CPLD code listing and the related registers refer to *section 1.10, "CPLD"*.

Figure 9-1. CPLD code listing

```
--*********************************************************************************--
--                    CPLD for the Taihu405EP Evaluation Board Ver10                --
--*********************************************************************************--
--*************** CPU R/W PORT, CPU STRAPPING, CONTROL SIGNALS ***************--
--*********************************************************************************--

LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY Taihu405EP_CPLD IS
PORT
    (
--  RESET SIGNALS
    RESET                   : IN STD_LOGIC;       -- RESET BUTTON INPUT
    PHY_RESET               : OUT STD_LOGIC;      -- ETHERNET PHY RESET
    SYS_RESET               : INOUT STD_LOGIC;    -- CPU RESET
    PCI_CARDBUS_RESET       : OUT STD_LOGIC;      -- CARDBUS CONTROLLER RESET
--  CHIP SELECT, R/W, CLOCK, ADDRESS BUS, DATA BUS
    EBC_CS2                 : IN STD_LOGIC;
    EBC_CS3                 : IN STD_LOGIC;
    EBC_CS4                 : IN STD_LOGIC;
    EBC_WE                  : IN STD_LOGIC;
    EBC_OE                  : IN STD_LOGIC;
--  ////////
    EBC_CLK                 : IN STD_LOGIC;       -- 55.5MHz
--  ////////
    EBC_A                   : IN STD_LOGIC_VECTOR(4 to 7);
    EBC_D                   : INOUT STD_LOGIC_VECTOR(0 to 7);
--  16245 BIDIRECTIONAL TRANSCEIVER OUTPUT ENABLE, LCM ENABLE
    T245_OE                 : OUT STD_LOGIC;
    LCM_E                   : OUT STD_LOGIC;
--  USER SWITCH, USB SUSPEND DETECT, USB RESET, LCM BACKLIGHT CONTROL
    SWITCH_STS              : IN STD_LOGIC_VECTOR(0 to 3);
    USB_SUSPEND             : IN STD_LOGIC;
    USB_RESET               : OUT STD_LOGIC;
    LCM_CTRL                : OUT STD_LOGIC;
```

```
--    CPU STRAPPING
      CPLD_UART1_TX          : IN STD_LOGIC;
      CPLD_UART1_RTS         : IN STD_LOGIC;
      CPLD_SYS_ERROR         : IN STD_LOGIC;
      PCI_M66EN_hardwire     : IN STD_LOGIC;
      UART1_TX               : OUT STD_LOGIC;    -- TRI-STATE OUTPUT
      UART1_RTS              : OUT STD_LOGIC;    -- TRI-STATE OUTPUT
      SYS_ERROR              : INOUT STD_LOGIC;
      SYS_ERROR_L            : OUT STD_LOGIC;
--    PCI SLOT 66MHz DETECT
      PRSNT1                 : IN STD_LOGIC;
      PRSNT2                 : IN STD_LOGIC;
      M66EN                  : IN STD_LOGIC;
      PCI_M66EN              : OUT STD_LOGIC;
      PCI_M33EN              : OUT STD_LOGIC;
--    JTAG PORT RESET
      JTAG_TRST              : IN STD_LOGIC;
      CPLD_TRST              : OUT STD_LOGIC
      );
END Taihu405EP_CPLD;


ARCHITECTURE RTL OF Taihu405EP_CPLD IS

SIGNAL PCI_M66EN_TMP : STD_LOGIC;

SIGNAL EBC_CS2_TMP : STD_LOGIC;

SIGNAL BOARD_RESET : STD_LOGIC;

SIGNAL VER : STD_LOGIC_VECTOR(0 TO 1);

SIGNAL REG0,REG1 : STD_LOGIC_VECTOR(0 TO 7);


BEGIN

VER <= "10";

--    RESET
PROCESS (RESET)
BEGIN

      IF RESET = '0' THEN
```

```
            SYS_RESET <= RESET;
        ELSE
            SYS_RESET <= 'Z';
        END IF;

END PROCESS;
BOARD_RESET <= RESET AND SYS_RESET;
PHY_RESET <= BOARD_RESET;
PCI_CARDBUS_RESET <= BOARD_RESET;

--    T245_OE
PROCESS (EBC_CLK)
BEGIN

        IF EBC_CLK'EVENT AND EBC_CLK = '1' THEN
                EBC_CS2_TMP <= EBC_CS2;
        END IF;

END PROCESS;
T245_OE <= EBC_CS2 AND EBC_CS2_TMP AND EBC_CS3 AND EBC_CS4;

--   LCM_E, EBC_A(6) = 1, LCM ENABLE
LCM_E <= NOT ((EBC_CS3 OR EBC_WE) AND (EBC_CS3 OR EBC_OE)) AND EBC_A(6);

--    SYS_ERROR_L, SYSTEM ERROR LED INDICATOR
SYS_ERROR_L <= NOT SYS_ERROR;

--   PCI 66MHz ENABLE
PCI_M66EN_TMP <= NOT (PRSNT1 AND PRSNT2) AND M66EN AND PCI_M66EN_hardwire;

PCI_M66EN <= PCI_M66EN_TMP;
PCI_M33EN <= NOT PCI_M66EN_TMP;

--    JTAG PORT RESET
CPLD_TRST <= JTAG_TRST AND BOARD_RESET;

--    CPU WRITES CPLD REGISTER1: REG1(0 TO 7)
PROCESS (BOARD_RESET,EBC_CLK)
BEGIN

        IF BOARD_RESET = '0' THEN
            REG1(6 TO 7) <= "01";        --   LCM_CTRL & USB_RESET
        ELSIF EBC_CLK'EVENT AND EBC_CLK = '1' THEN
            IF EBC_CS3 = '0' AND EBC_WE = '0' AND EBC_A(6 TO 7) = "01" THEN
```

```
                REG1(6) <= EBC_D(6);
                REG1(7) <= EBC_D(7);
            END IF;
        END IF;

END PROCESS;

REG1(0 TO 5) <= "000000";               -- RESERVED
LCM_CTRL <= REG1(6);                    -- LCM_CTRL
USB_RESET <= REG1(7) AND BOARD_RESET;           -- USB_RESET

--      CPU READS CPLD REGISTER0,REGISTER1: REG0(0 TO 7), REG1(0 TO 7)
REG0 <= VER & USB_SUSPEND & PCI_M66EN_TMP & SWITCH_STS;


PROCESS (EBC_CS3,EBC_OE,EBC_A(6 TO 7),REG0,REG1)
BEGIN

        IF EBC_CS3 = '0' AND EBC_OE = '0' AND EBC_A(6) = '0' THEN
            IF EBC_A(7) = '0' THEN
                EBC_D <= REG0;
            ELSE
                EBC_D <= REG1;
            END IF;
        ELSE
            EBC_D <= (OTHERS => 'Z');
        END IF;

END PROCESS;

--    CPU STRAPPING
PROCESS (BOARD_RESET,CPLD_UART1_TX,CPLD_UART1_RTS,CPLD_SYS_ERROR)
BEGIN

        IF BOARD_RESET = '0' THEN
            UART1_TX <= CPLD_UART1_TX;
            UART1_RTS <= CPLD_UART1_RTS;
            SYS_ERROR <= CPLD_SYS_ERROR;
        ELSE
            UART1_TX <= 'Z';
            UART1_RTS <= 'Z';
            SYS_ERROR <= 'Z';
        END IF;
```

```
END PROCESS;

END RTL;
```